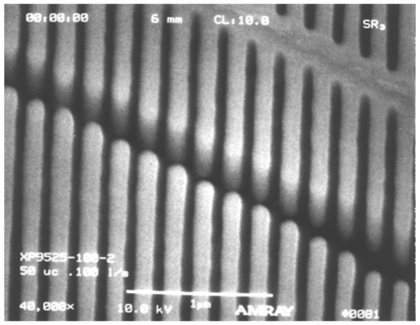
Mask Fabrication For Nanoimprint Lithography



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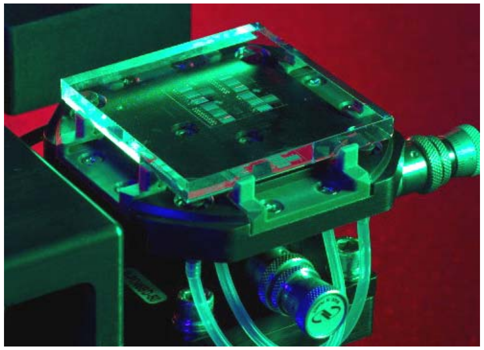

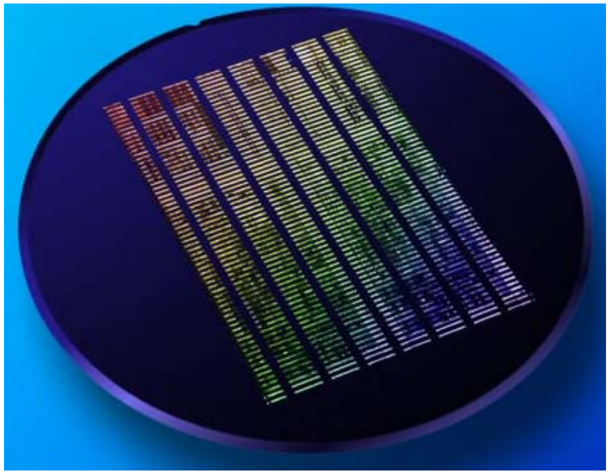

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Template (Imprint Mask) Fabrication: Outline

- E-beam and Etch Basics
- Thermal IL Template Fabrication Process
- Templates for Soft Lithography
- J-FIL Templates
  - Processing Challenges
  - Mask Shop Compatible Process
- Commercial Path for Templates
  - Gaussian based templates
    - Resolution and Line Width Roughness (LWR)
  - Variable Shape Beam templates
    - Resolution, Image Placement, Write Time
  - Mask Replication
    - Template Inspection
    - Template Repair
- Templates for full wafer/disk, and R2R imprinting
- Conclusions

By the end of the course, you will know how to fabricate (or better yet, order) your own templates

First, A Brief History Lesson

EUVL:	Started late 1980's
EPL:	Started ~ 1990
MBDW:	Started in the 1980's
193Immersion:	Started ~2001

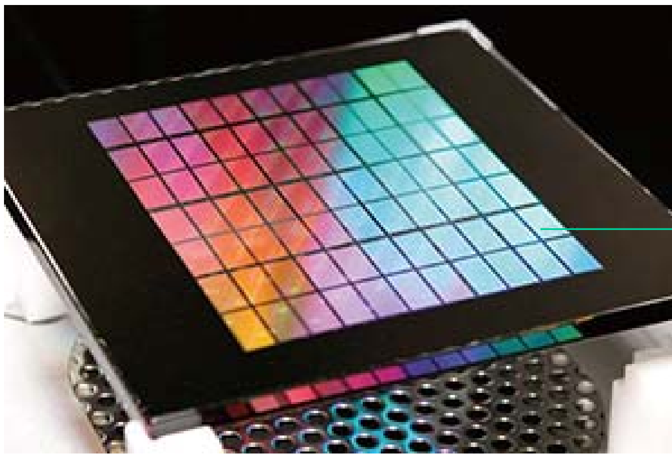
Gutenberg Press

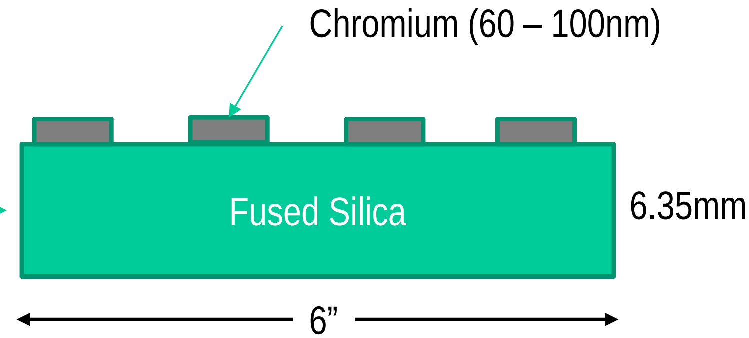
Imprint Lithography

1041 Movable clay type invented in China.
1436 Gutenberg commenced work on his press.
1440 Gutenberg completed his press which used metal moving type.
1455 Gutenberg completed work on his 42 Line Bible.
1455 Gutenberg was effectively bankrupt.
1456 Mazarw Bible printed in Mainz.
1462 The attack on Mainz by soldiers of the Archbishop of Nassau, caused printers to flee and spread their skills around Europe.
1477 The first book to be printed in England (by Caxton)
1499 Printing established in more than 250 cities in Europe.

Mask Basics

Photomask





• For a photomask, light is projected through the mask, through a lens (with 4x reduction optics) and an aerial image is projected into a photoresist on a silicon wafer

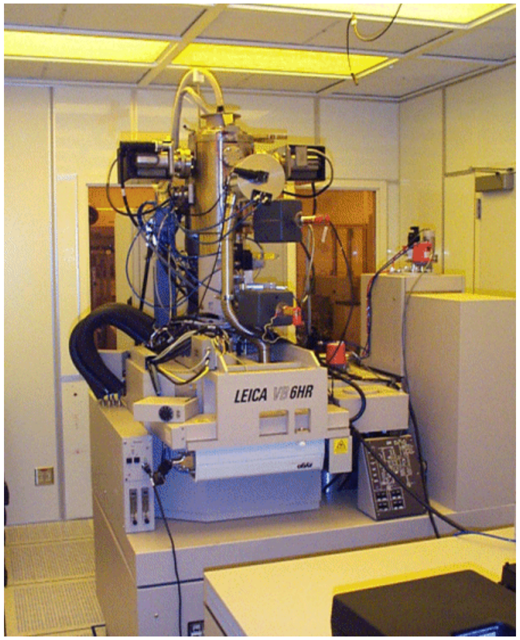
• For an imprint mask (or template), the final resist image depends almost entirely on the relief feature on the template

Template Fabrication

Fabrication of a template generally requires:

- Patterning of a resist (Electron beam writing system)
- Pattern transfer of the pattern into an underlying material (RIE)

E-beam Systems



Gaussian-Beam tool

Shaped-Beam Tool

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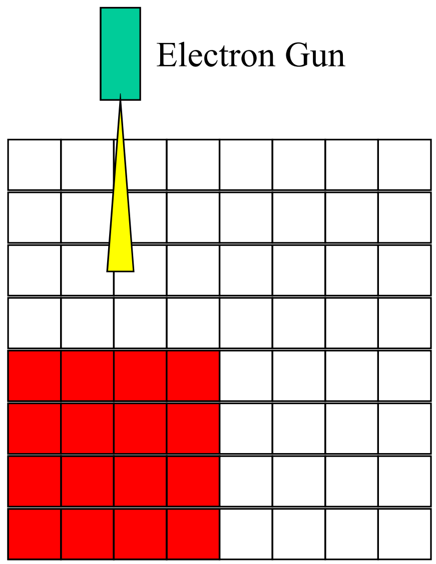
Electron Beam Writing Strategies

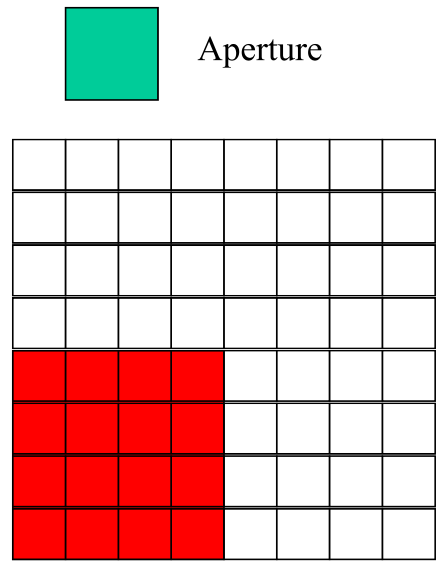
Gaussian Beam



<u>Pros and Cons</u>

- Small spot size
- Dreadfully slow
- Example: Vistec VB300

Shaped Beam

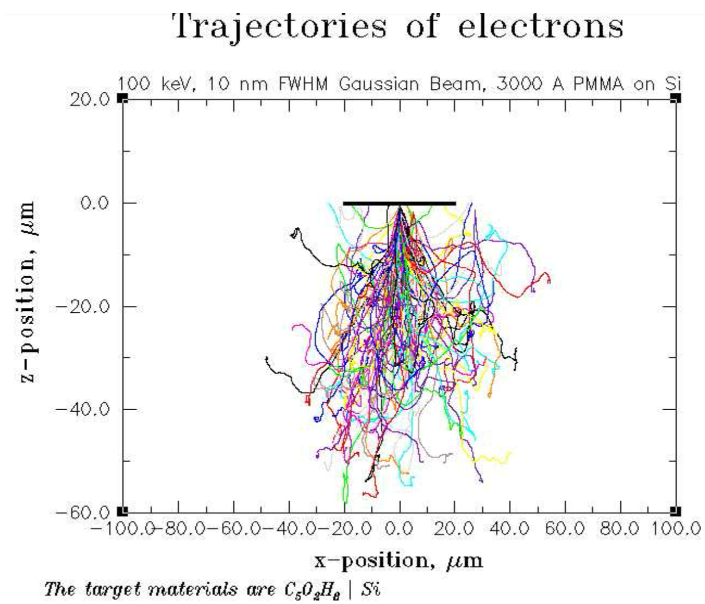


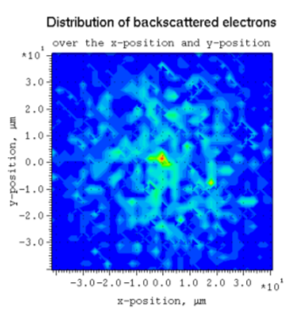
<u>Pros and Cons</u>

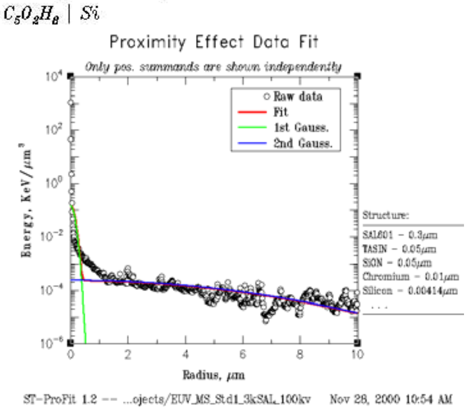
- Much faster
- Resolution limited by blur
- Example: NuFlare EBM 7000

Electron Scattering Basics

(Subtitle: Why electron beam lithographers are unhappy people)



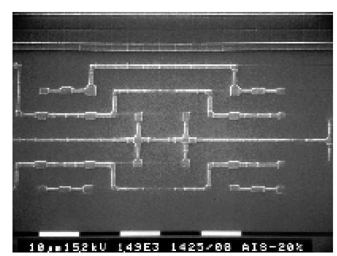




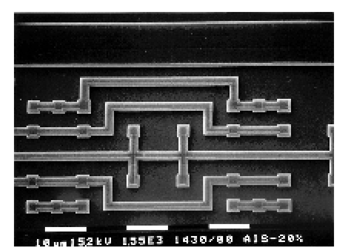
Proximity Correction

$$M(r) = \frac{1}{\pi(1+\eta)}\left[\frac{1}{\alpha^2}\exp\left(-\frac{r^2}{\alpha^2}\right) + \frac{\eta}{\beta^2}\exp\left(-\frac{r^2}{\beta^2}\right)\right]$$

α-forward scattering coeff.
β-backscattering coeff.
η-ratio of backscattering to forward



Uncorrected



Proximity Corrected

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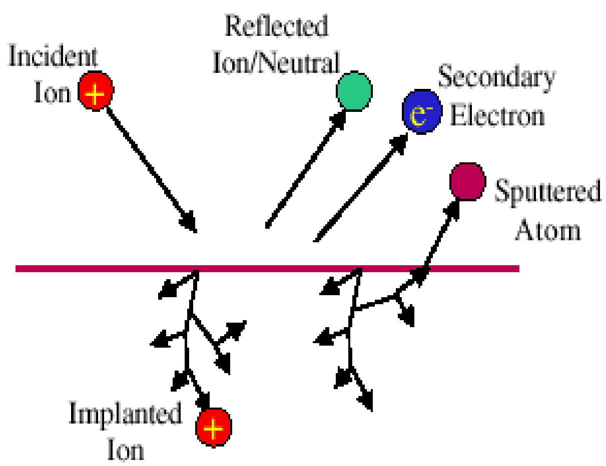
Etch Basics: Sputtering

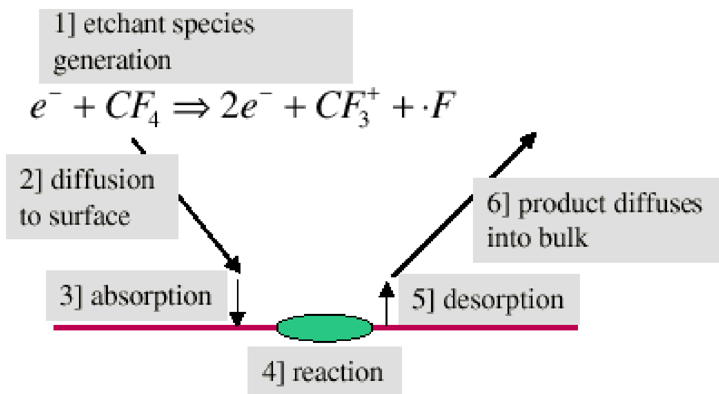


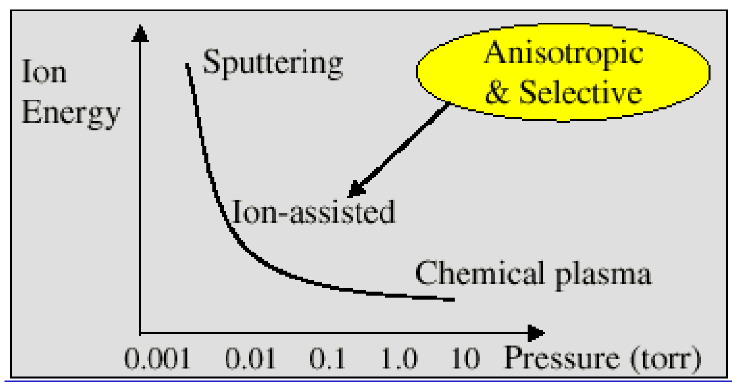
Ion Energy (eV)	Reaction
<3	Physical absorption
4 -10	Surface sputtering
10 - 5000	Sputtering
10,000 - 20,000	Implantation

- **Sputtering has an angular dependence (faceting).**
- **Sputtering reduces the need for product volatility.**
- **Sputtering provides directional anisotropy.**
- **Inert gases provide good yields and avoid contamination.**
- **Redeposition is an issue.**
- **Aspect ratio is limited.**

**After Berkeley Labs*

Etch Basics: Chemical Etching



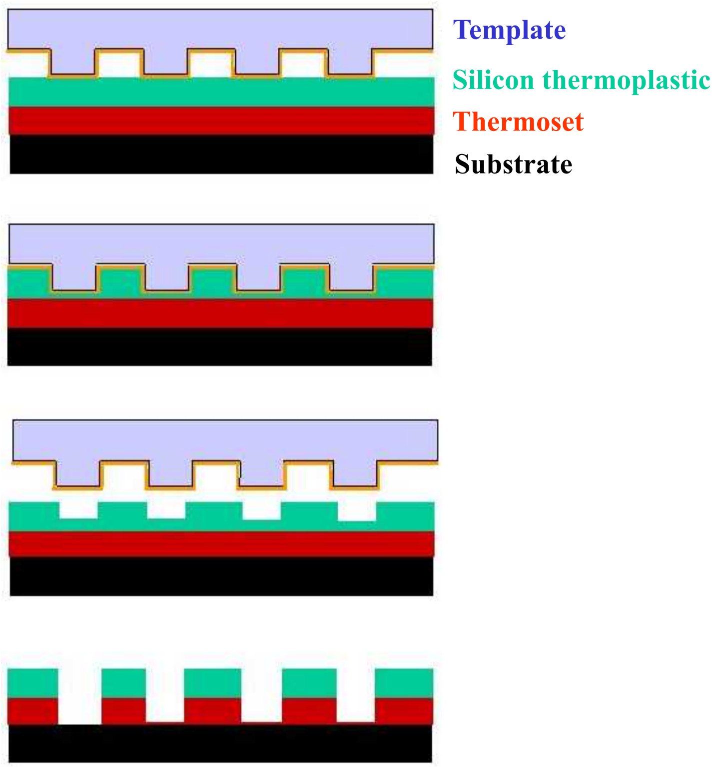


- **At higher pressures, substrate removal is accomplished primarily by reactive species generated in the plasma.**
- **Reaction rate can be strongly influenced by ions**
  - damage
  - clean
  - energy for reaction
- **Low pressure results in normal ion incidence, but also typically lower ion densities.**
  - A variety of tool configurations are available on the market to address specific applications.

**After Berkeley Labs*

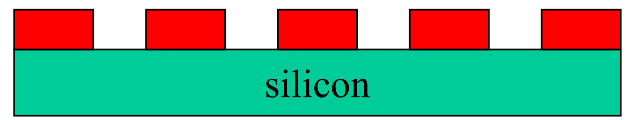
Thermal IL Template Fabrication

Thermal IL Process

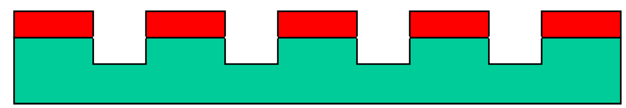


S. Chou, Princeton

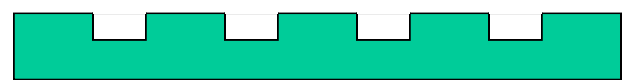
The most common IL template is simply a patterned silicon wafer



E-beam pattern resist



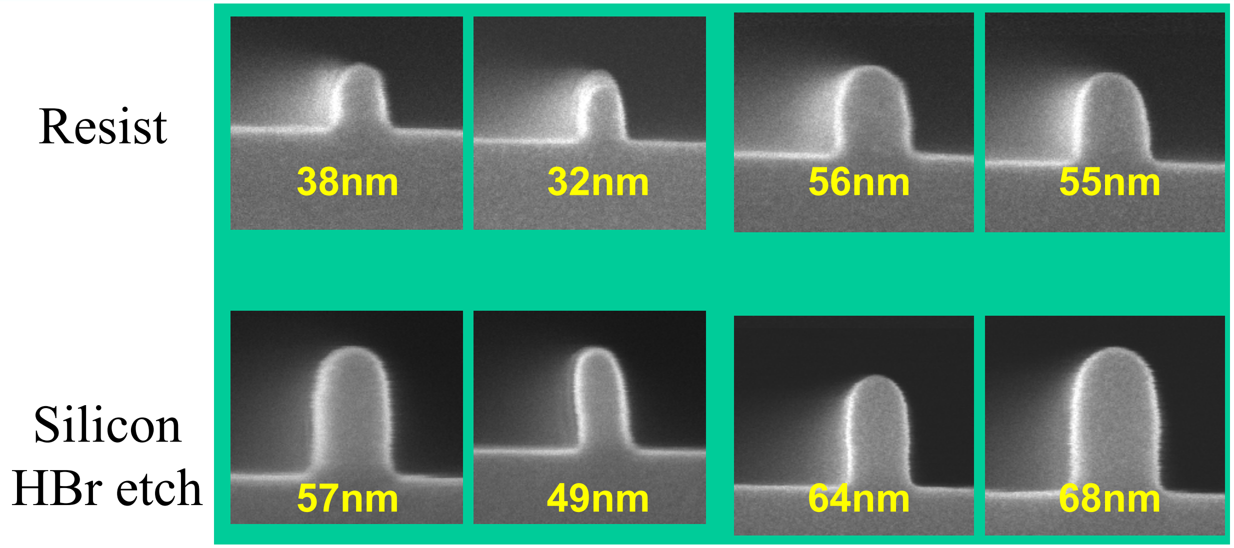
Etch silicon



Strip Resist

Silicon can be etched with SF_6, CF_4, Cl_2, HBr, etc…

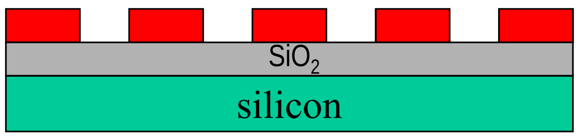
Silicon Etch



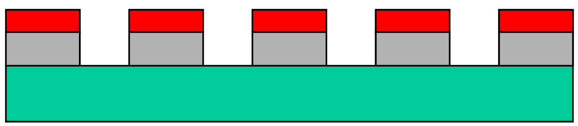
- Cl_2 and HBr chemistries tend to etch silicon more anistropically
- SF_6 and $CF_4/0_2$ tend to undercut the feature (end product is SiF_4)
- Resist alone is not always a sufficient etch mask. Oxides, nitrides, and chrome are often used as hard masks

IL Template Fabrication

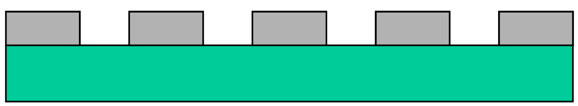
Another popular IL template scheme uses SiO_2 as the mold



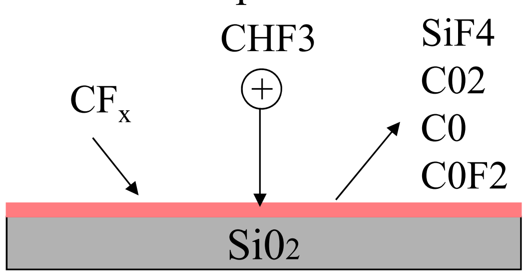
Pattern resist



Etch oxide

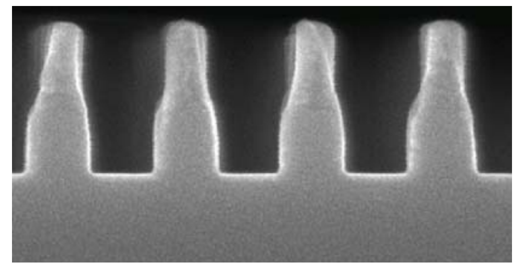


Strip Resist

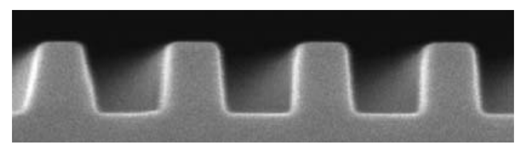


Ion enhanced reaction, selective to Si

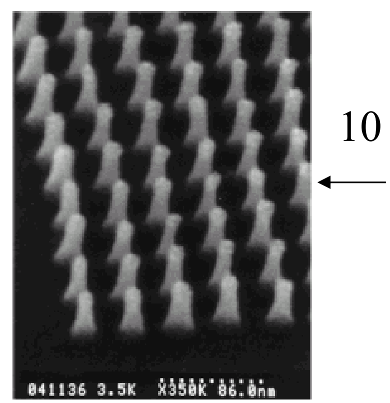
* Plasma Etching: Daniel Flamm



After SiO_2 etch



After resist strip



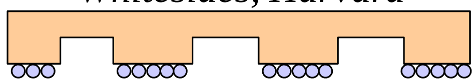
10 nm $Si0_2$ pillars on silicon

*from Chou

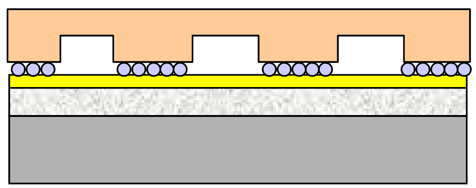
Soft Lithography Templates

Soft Lithography

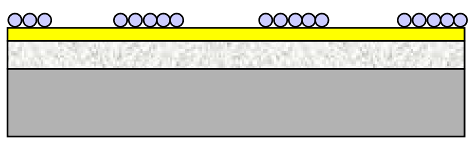
Whitesides, Harvard



1. PDMS template with thiol



2. Imprint stamp

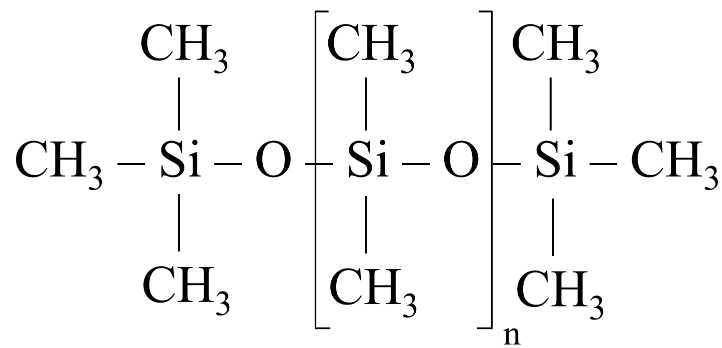


3. Transfer molecules

4. Pattern Transfer

Polydimethylsiloxane (PDMS)

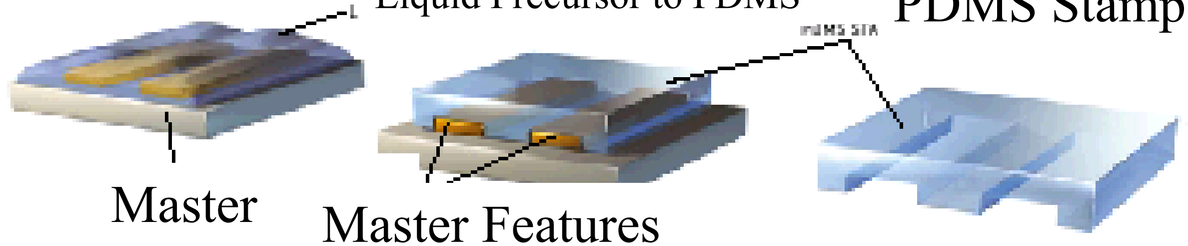
Elastomeric material: polymer chain of silicon containing oils

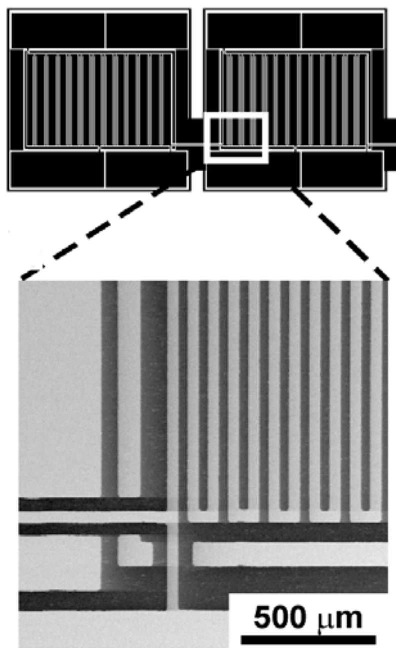


Example: Sylgard 184: Dow Corning

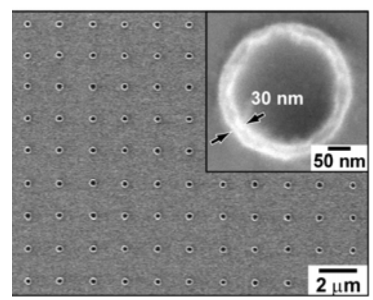
Tensile strength:	7.1 MPa
Elongation at break:	140 %
Tear strength:	2.6 kN/m

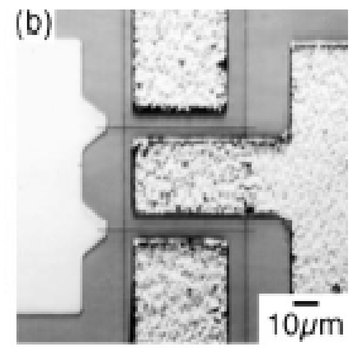
PDMS Fabrication Process





Microfluidic device





FET

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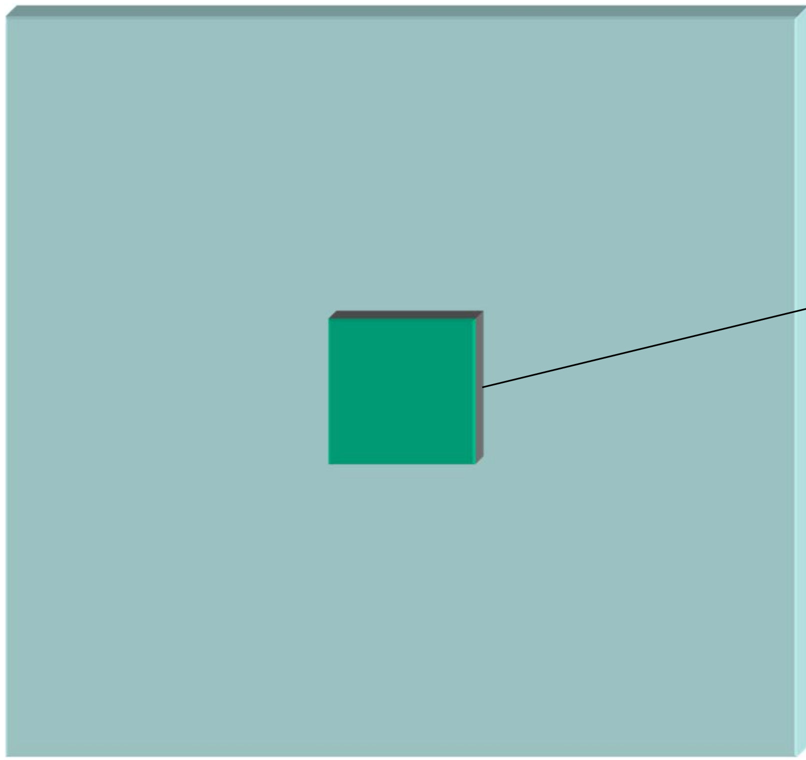
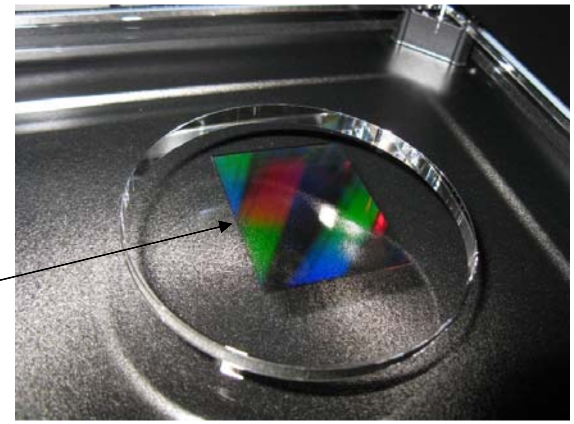
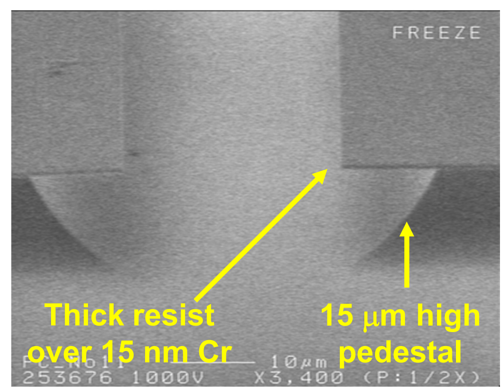
J-FIL Template Layout for Semiconductors



6” x 6” x 0.25” (6025) quartz blank substrate
Patterned area rests on a mesa (15-30um)

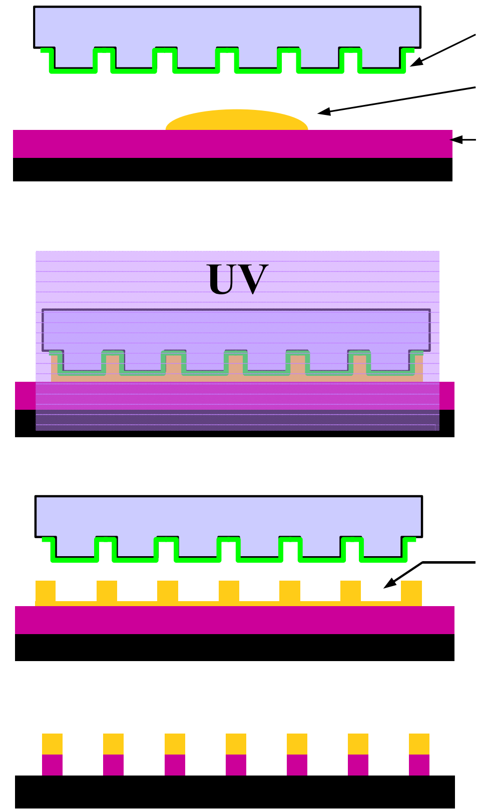
26mm x 33mm Patterned area





J-FIL Template Attributes

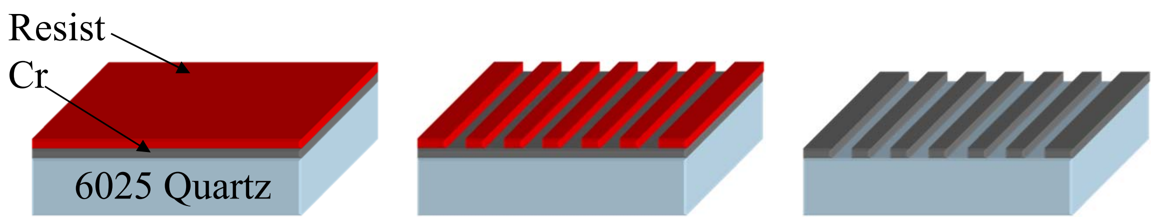
J-FIL Template



Template Attributes:

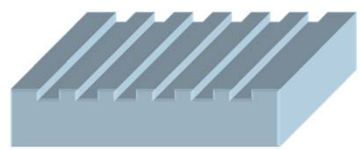
- Transparent to UV light
- Compatible with a release layer
- Compatible with alignment schemes
- Mechanically durable
- Chemically durable (cleaning)
- Manufacturable
  - ***Good CD control***
  - ***Good Image Placement***
  - ***Low Defectivity***
  - ***Inspectable: UV, DUV, e-beam***
  - ***Repairable***

Conventional Photomask Processing



Resist applied to 80 nm of Cr — Expose/develop e-beam resist — Etch chrome (wet or dry), strip resist

To fabricate a J-FIL Template, we need to add one more step



Etch quartz,
Strip chrome

This process is currently used in mask shops to fabricate phase shift masks

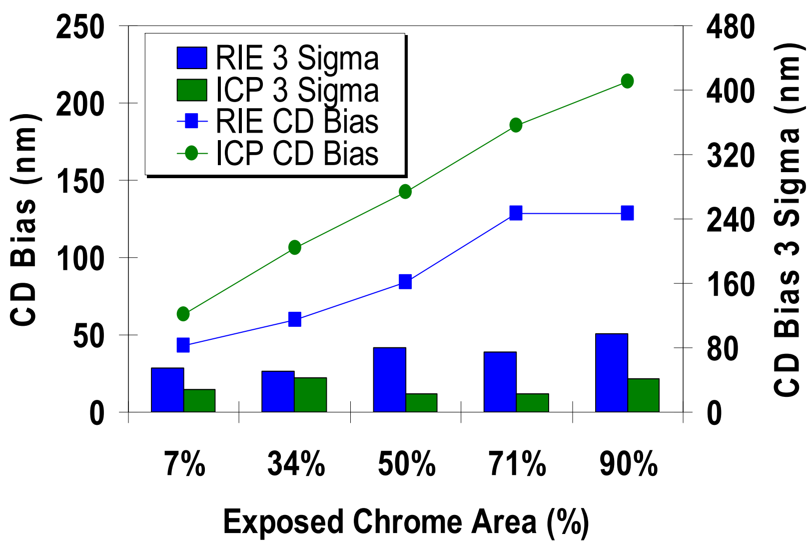
<u>So, What's the Problem?</u>

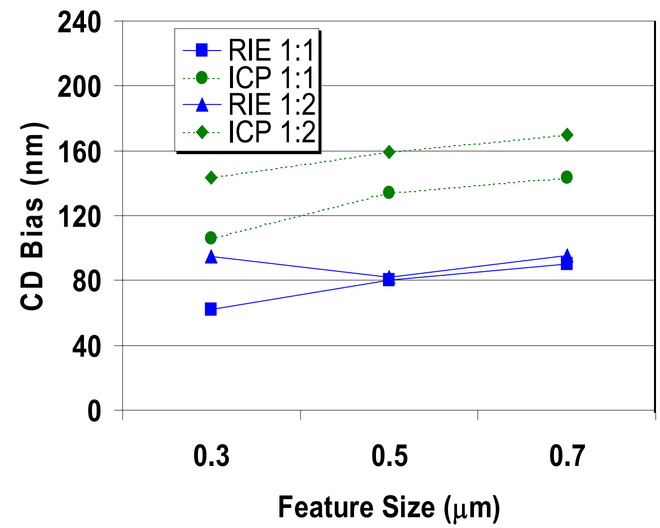
- We're making 1X masks, so we must dry etch
- Dry etching of Cr is subject to undercut and loading effects

Chromium Etching

$$Cr + 2O^* + 2Cl^* \rightarrow CrO_2Cl_2$$

<u>Issues:</u> The etch has a large chemical component: undercut
The process requires a lot of oxygen (25%): resist loss
The process is subject to loading effects: CD variation





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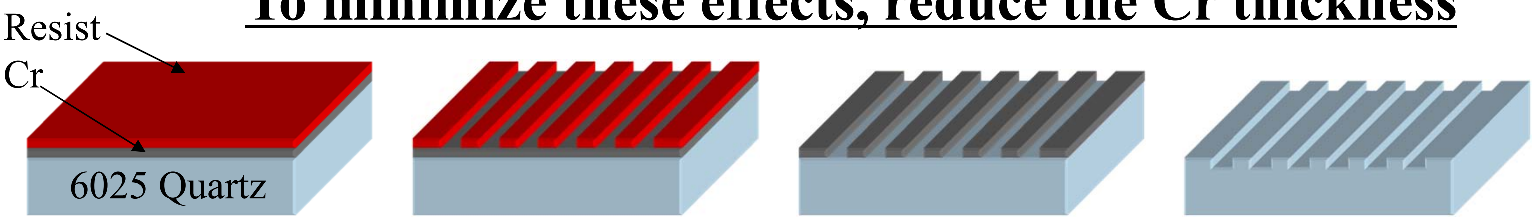
J-FIL Template Fabrication Schemes

To minimize these effects, reduce the Cr thickness



Resist applied to <15 nm of Cr	Expose/develop e-beam resist, descum	Etch chrome, strip resist	Etch quartz, Strip chrome

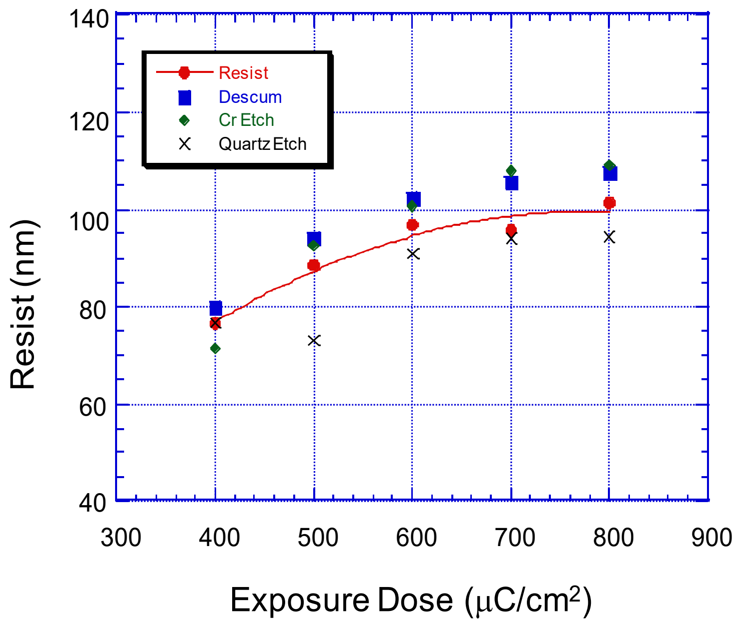
- **Compatible with existing Mask Shop Processes**

Following Slides:

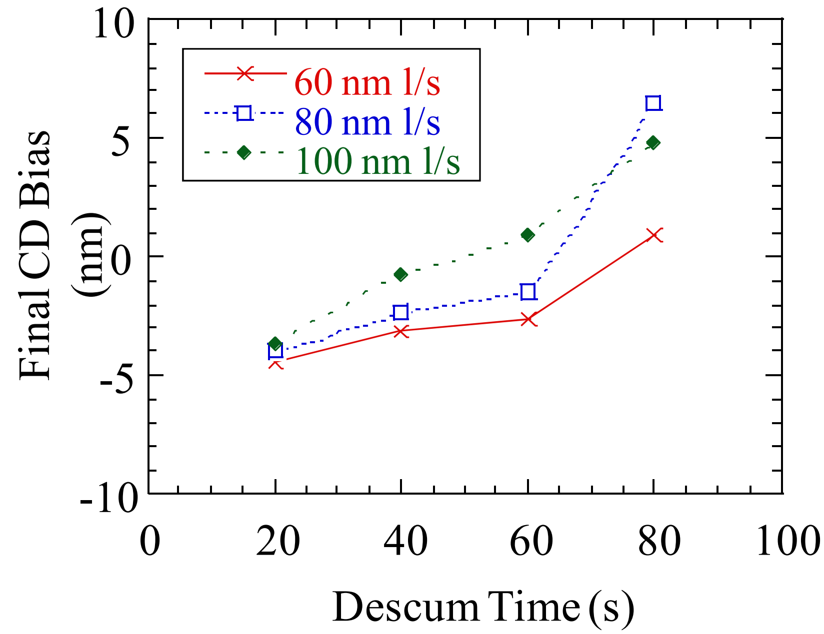
- Leica VB6 operating at 100 kV
- 5 nm address grid
- ZEP520 positive e-beam resist
- Track processing on an EVG 150/160
- Etching: Unaxis VLR
- Gas Chemistry: Cr – Cl_2/O_2, SiO_2 – CF_4/O_2

ZEP520 Exposure/Descum

ZEP520A process latitude is excellent



2.6nm change for every 20 seconds



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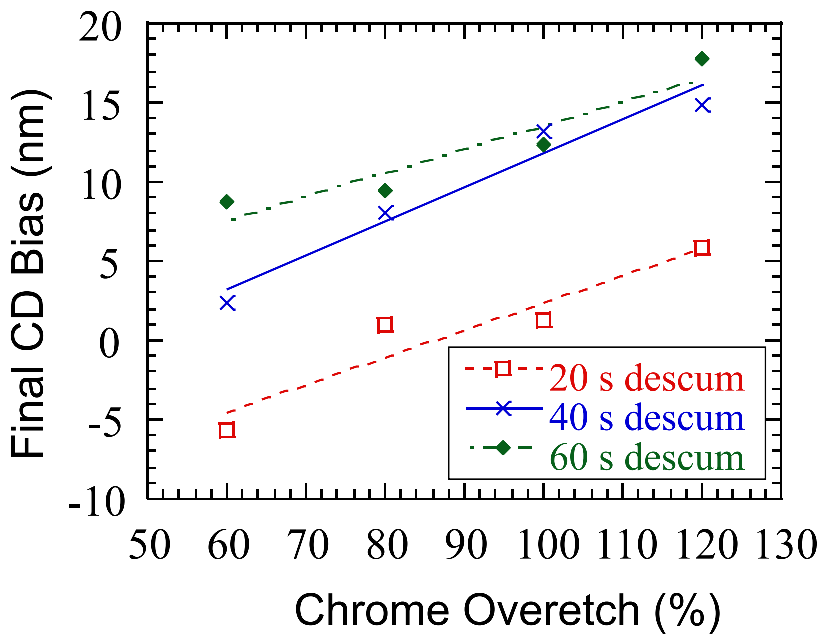
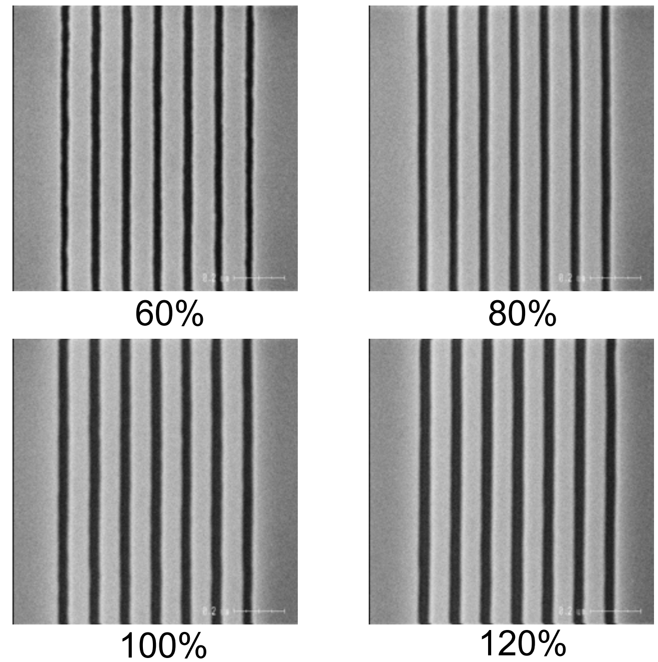
Cr Process CD Results





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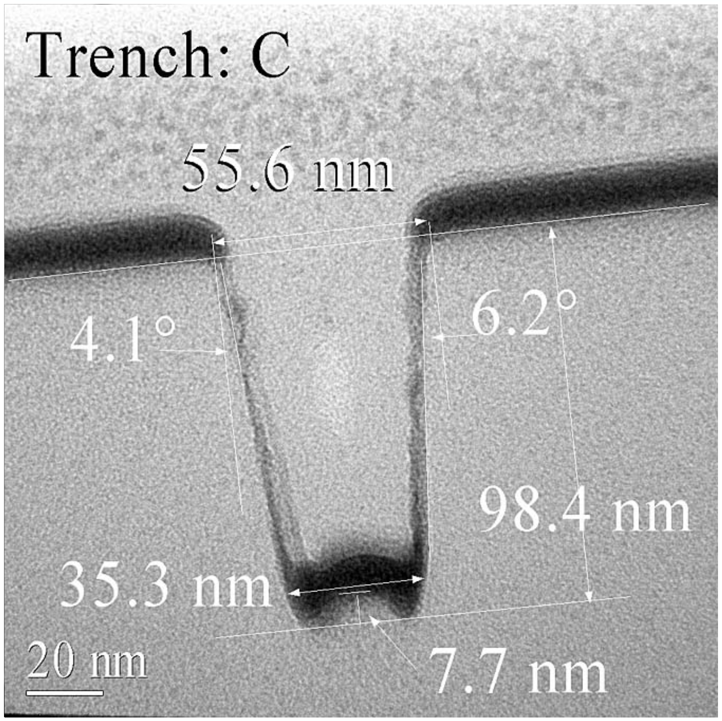
- All results shown are for 80 nm features.
- Similar to observations made for increasing descum time, a positive CD change of 3.8 nm per 20% of Cr overetch exists.

FIB/TEM Feature Profile



PF030323-3.4

- Cross-sectioning the trenches was done using a focused ion beam tool in conjunction with a protective film stack to avoid extreme charging, sample drift, and surface damage.

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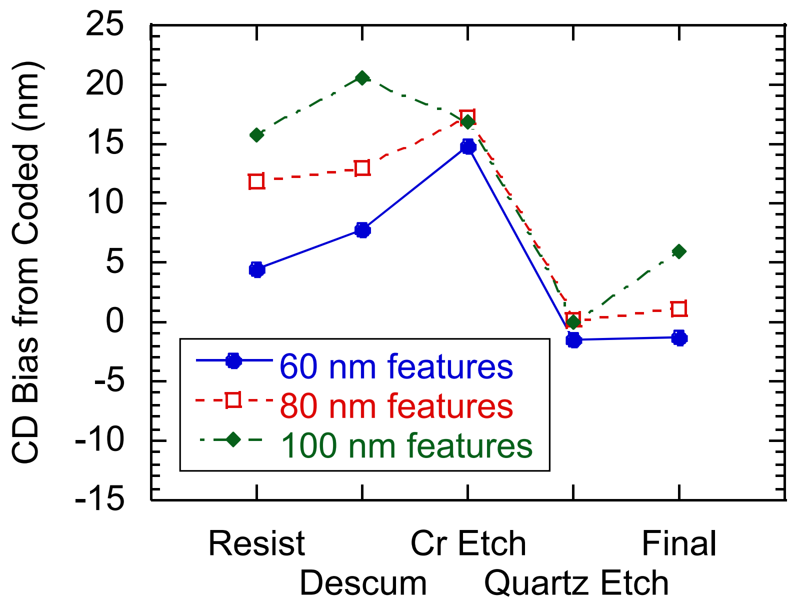
- Using TEM measurements as a basis, sidewall angles of 150 nm features were calculated to be ~ 84°
- The measured etch depth of 98 nm compares extremely well to profilometer and AFM measurements.

Fabrication Window

- A 20 s descum coupled with a 110% Cr overetch was found to give the best performance in terms of CD control and line edge roughness.



- For 60 nm clustered features, the spaces measure ~ 4 nm over coded size.
- The descum process increases CD by about the same magnitude.
- Resist erosion during Cr etch results in approximately 7 more nanometers of bias.
- After quartz etch, CD bias is 1.5 nm less than coded. The quartz sidewall angle is about 5° from the normal
- Final CD bias ends up approximately 1 nm from coded after the Cr hardmask is stripped.

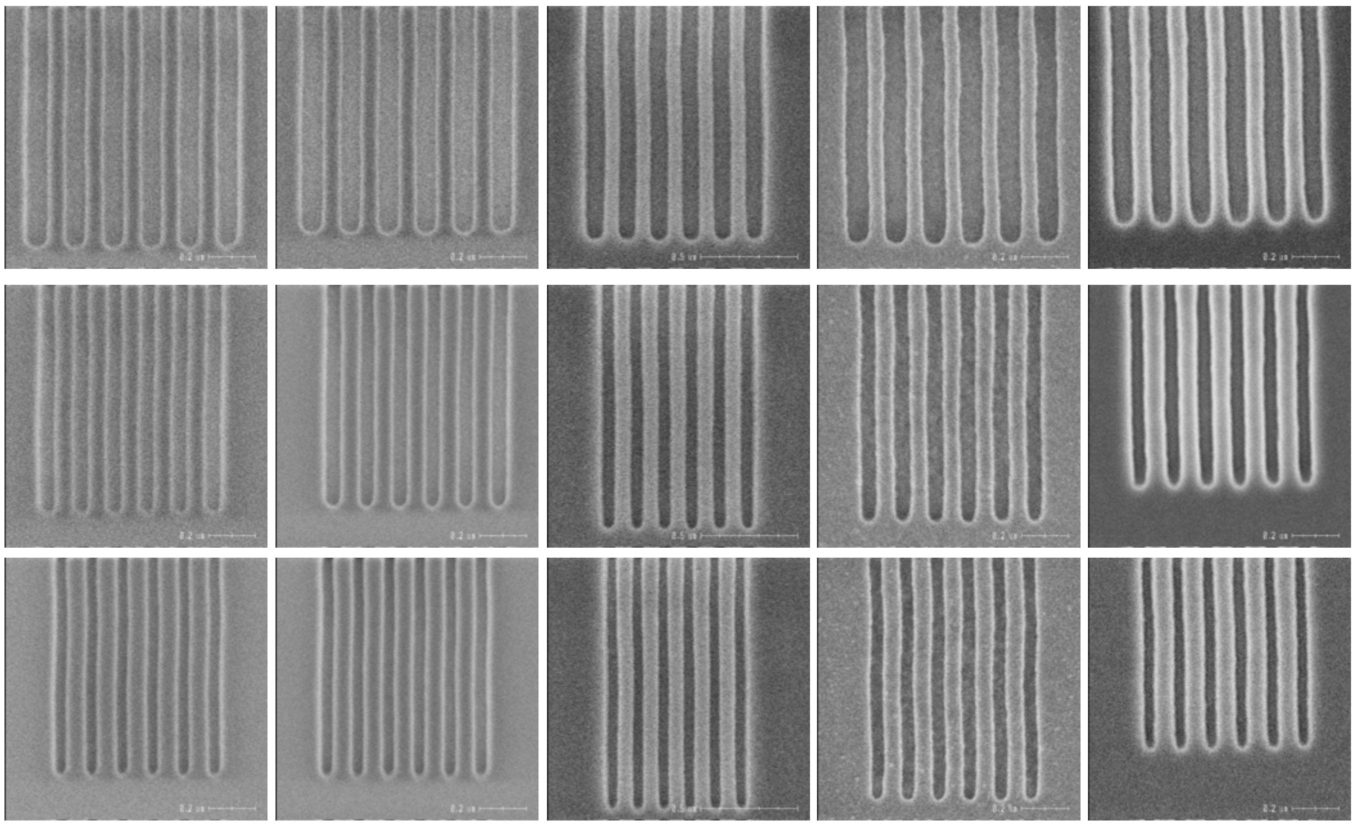
Pattern/Pattern Transfer Process

Resist | Descum | Cr Etch | Resist Strip | Quartz Etch

60 nm

40 nm

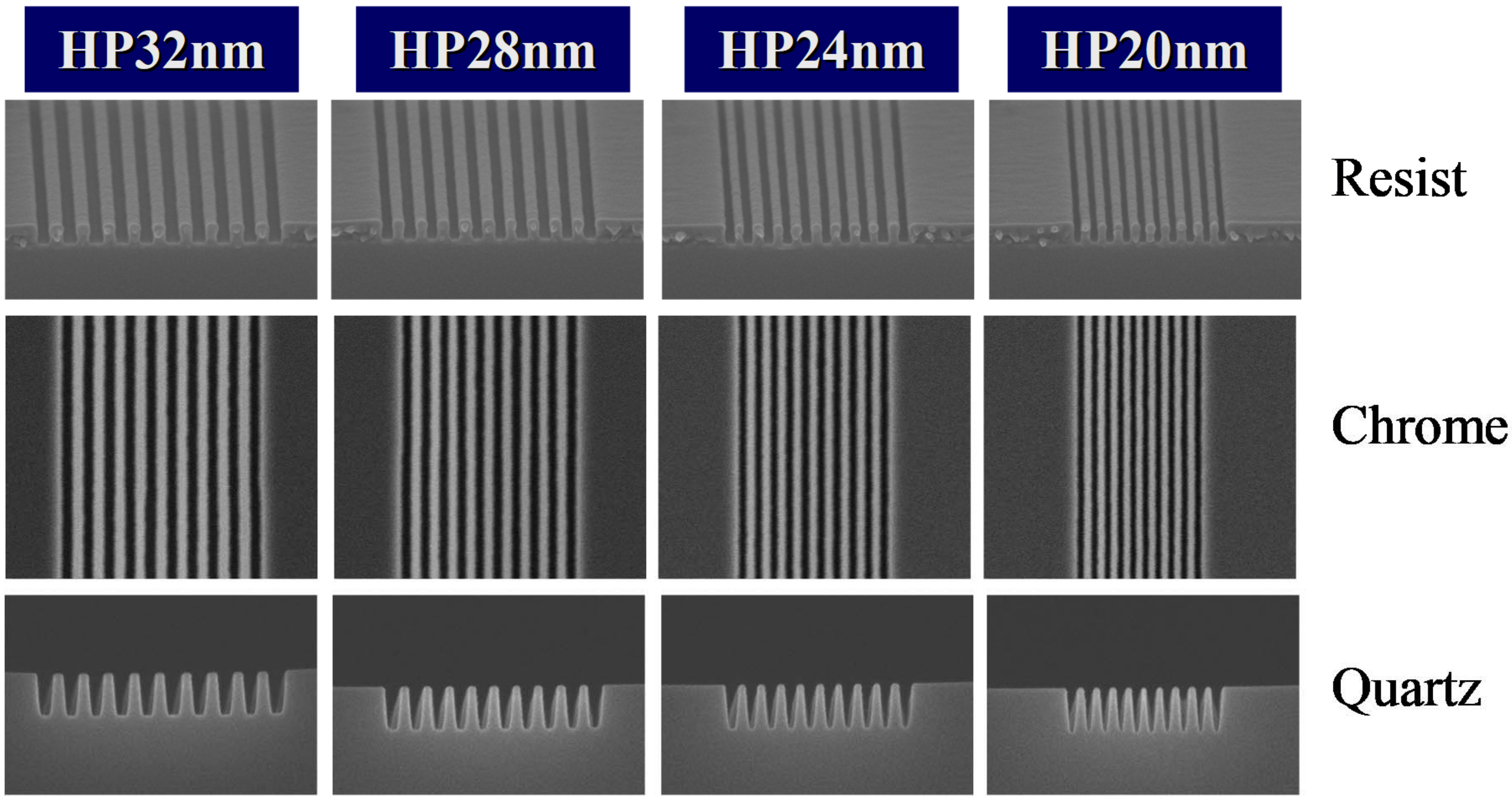
30 nm



Pattern Transfer Process

DNP

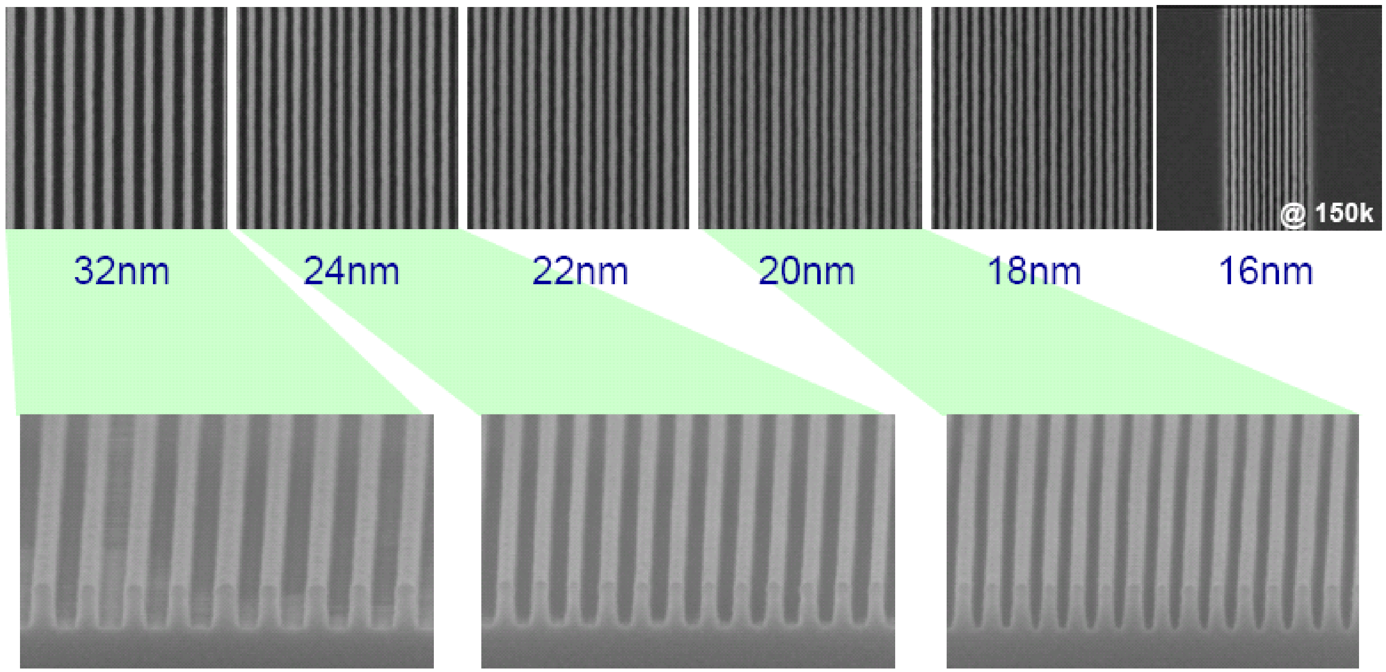
Magnification : 150k



Resolution with 100kV GB writer **DNP**

Magnification : 200k

Line&Space pattern 1/2Pitch



Etched quartz images

Electron Beam Pattern Generators

There are two methods for generating patterns on a template:

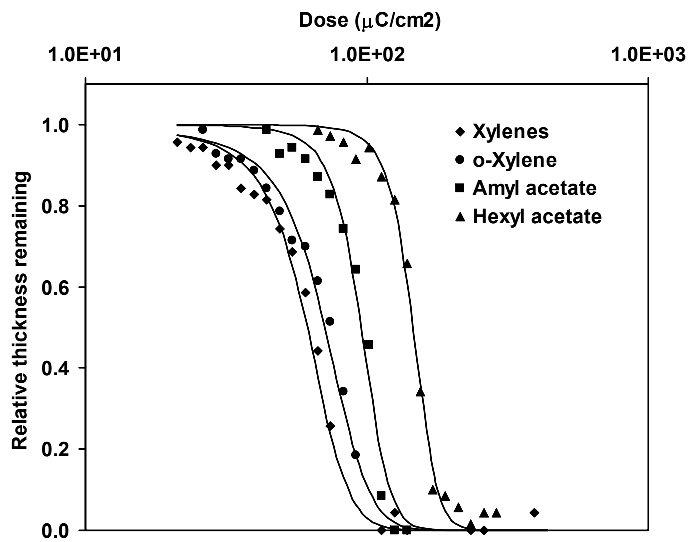
1. *<u>Gaussian beam PGs</u>: Great for unit process development and device prototyping*
2. *<u>Variable Shaped Beam PGs</u>: Needed for full field pattern generation and for image placement*

- **How do I get the best result from each tool?**
  - Resolution
  - Line Width Roughness
  - CD uniformity
  - Image Placement
  - Write Time

Gaussian Beam Pattern Generators

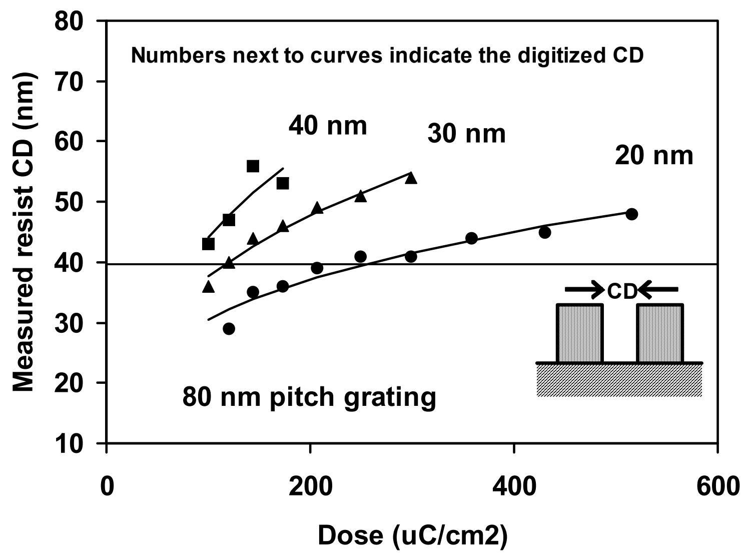
ZEP520A Process Development

- Resist response was studied for a variety of different developers



Amyl Acetate developer provides a good combination of contrast and sensitivity

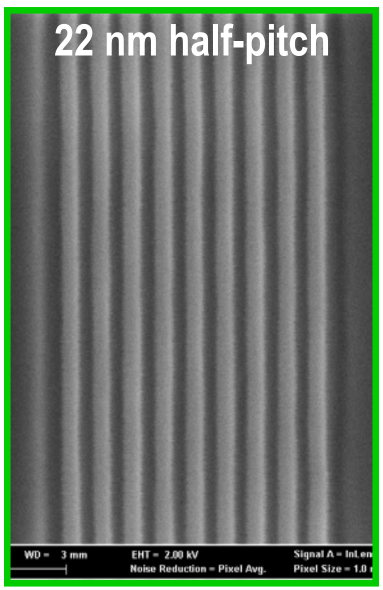
- Exposure latitude of the resist was mapped as a function of feature bias

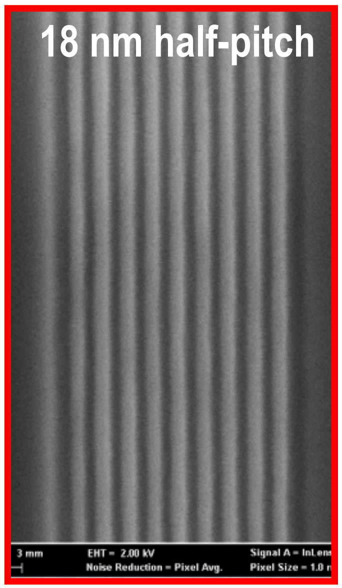


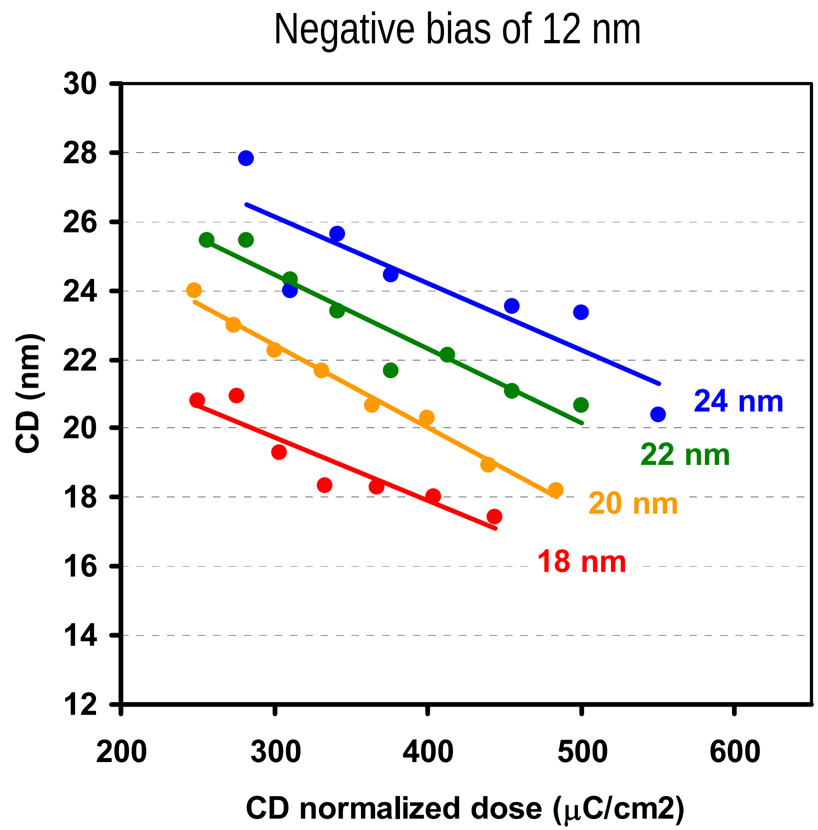
Exposure latitude is improves as biasing of critical features increases

Development of ZEP520A resist

- **Sonication of developer bath**
- **Dilution of developer**
  - *Equal mixture of amyl acetate with isopropyl alcohol*
  - *120 s puddle development*
  - *60 s isopropyl alcohol rinse, dry*

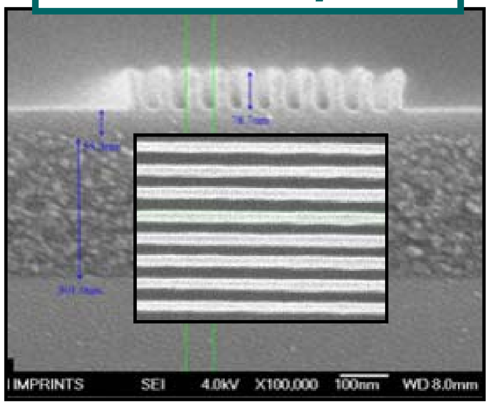




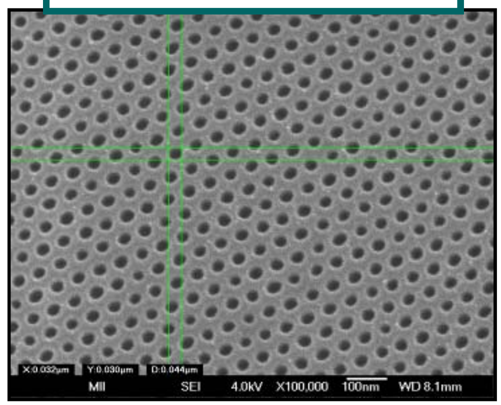


Imprint Resolution

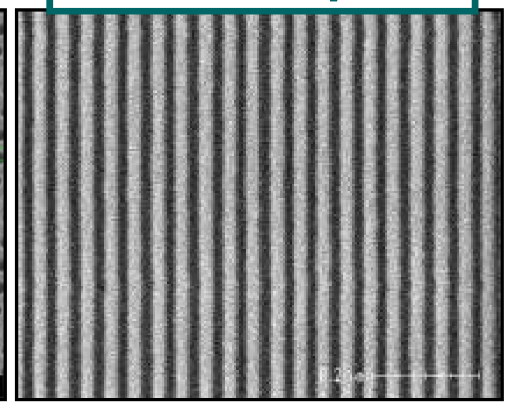
28nm half-pitch



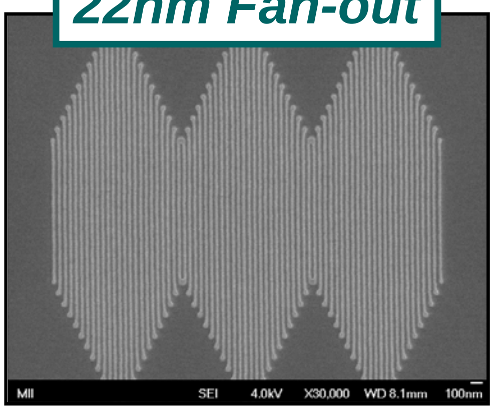
25nm Contacts



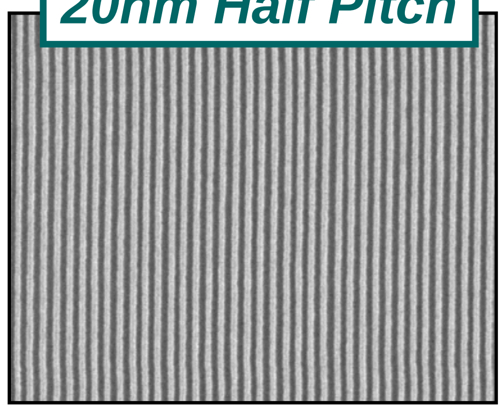
22nm half-pitch



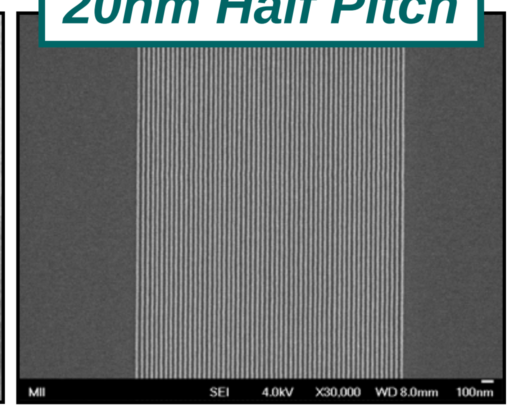
22nm Fan-out



20nm Half Pitch



20nm Half Pitch



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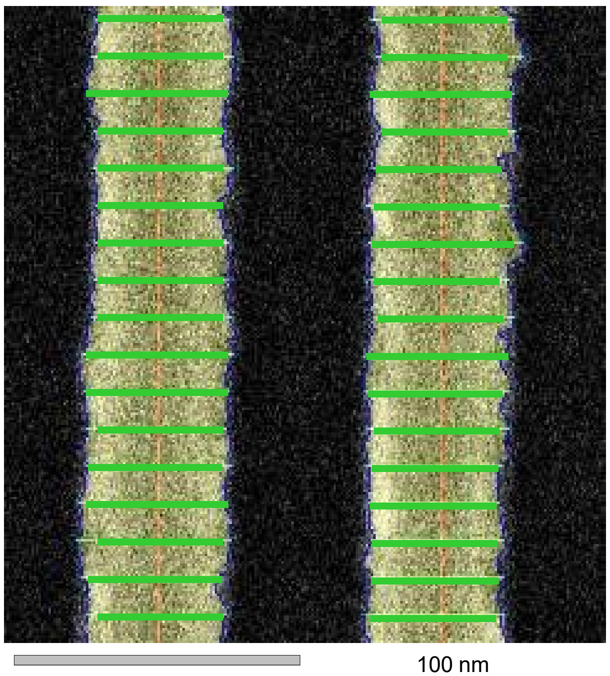
Line Width Roughness (LWR)

- **Variation in CD along the length of a line**
  - Results in variation of MOS gate width
  - Affects device speed of individual transistors
  - Leads to IC timing issues



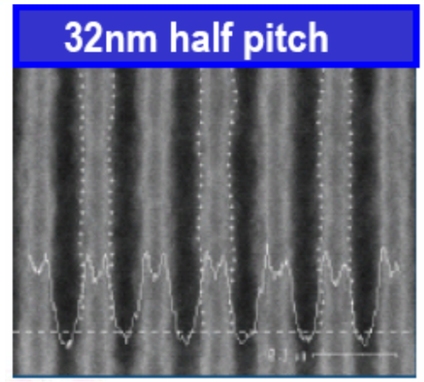
ITRS Roadmap for LWR (nm, 3σ)

	2007	2010	2013	2016	2019
DRAM Half-Pitch	65	45	32	22	16
LWR	3.4	2.4	1.7	1.2	0.8

Future nodes have no known solutions.

LWR Example: EUVL

- **Throughput requirements of EUVL require the use of fast chemically amplified resists**
  - Low exposure doses required for throughput
    - Too few photons: ~2 / nm^2
    - Shot noise effects

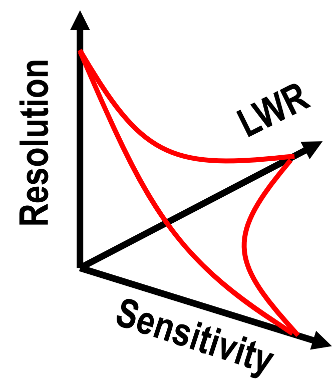


LWR ~ 6-8 nm
(SPIE)

- **RLS Trade-Off for Chemically Amplified Resists**

Resolution vs. LWR vs. Sensitivity

(Robert Brainard, Gregg Gallatin)



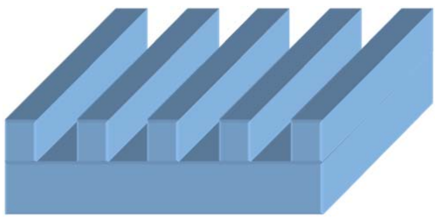
So, is imprint lithography immune to this problem?

YES! <u>And</u> NO!!

Pattern formation with J-FIL technology

Imprint Mask Fabrication

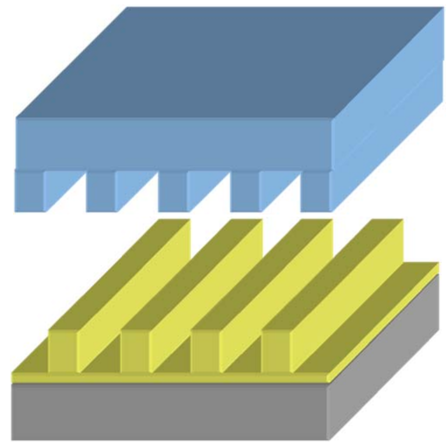
Resolution and LWR



- Use non-CA resists for best resolution and LWR performance.
- Utilize existing photomask infrastructure for fabrication and inspection.

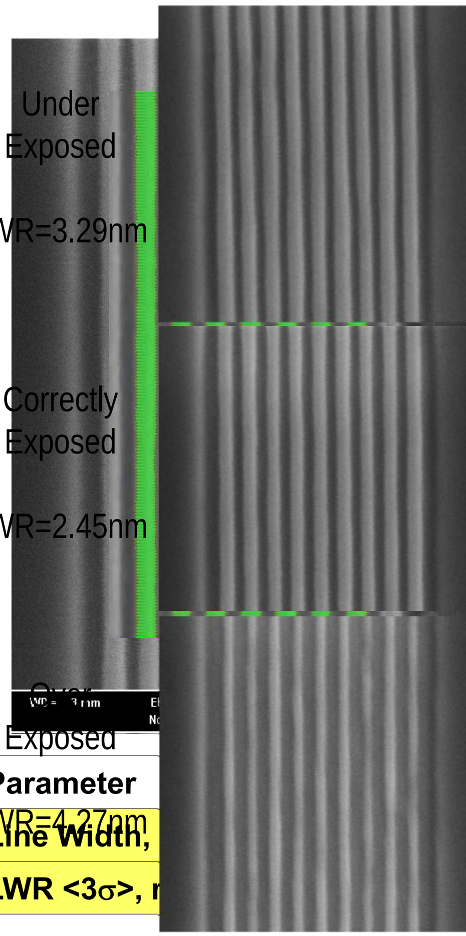
Imprint Patterning

Throughput



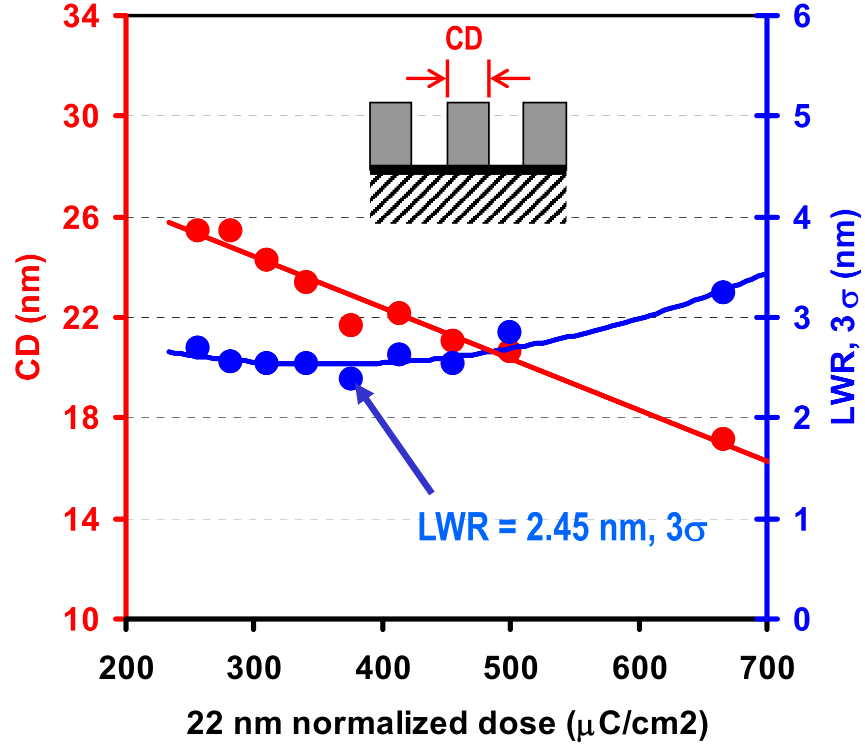
- CD, CDU, LWR, etc. of the patterned resist is determined by the template.

LWR minimization at 22 nm



Parameter
Line Width,
LWR <3σ>, r

22 nm HP



250 $\mu C/cm^2$: ~15 electrons / nm^2
Gaussian E-Beam exposure at 100kV

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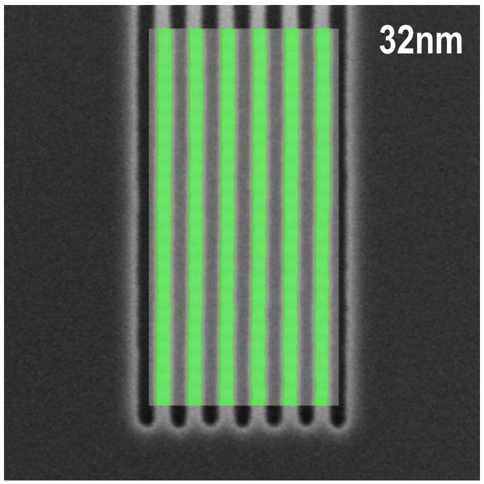
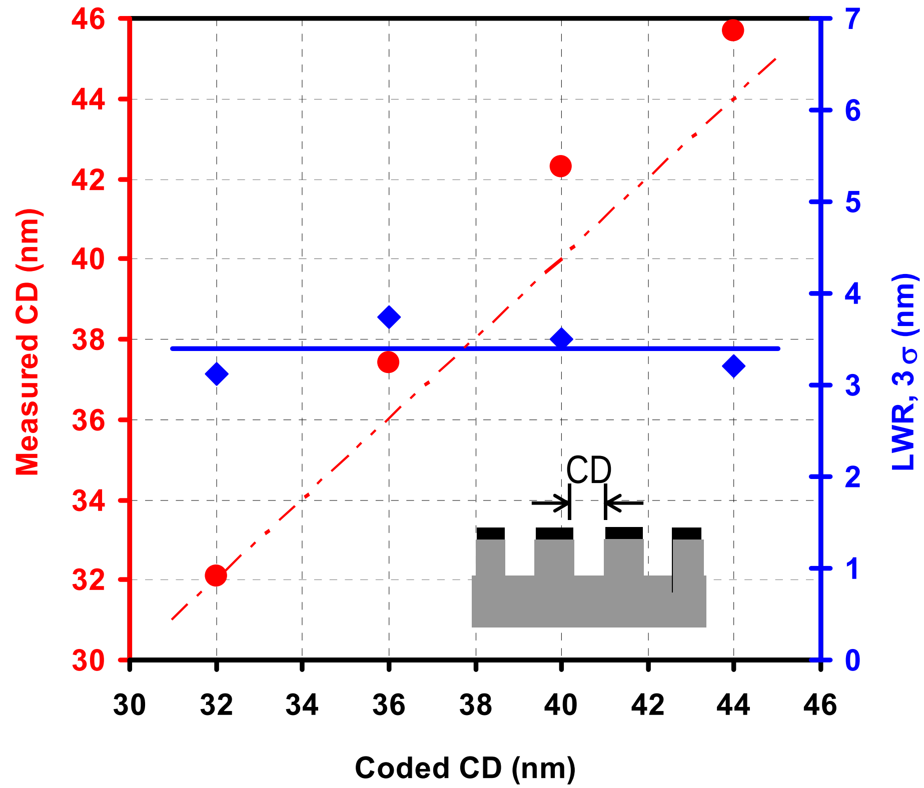
Template: CD and LWR Analysis

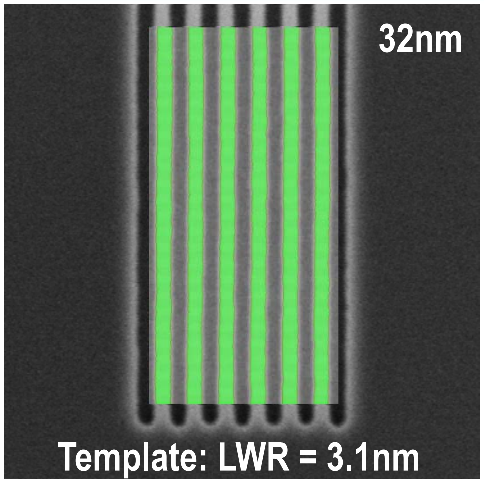


Parameter	Mean, nm	Std. dev., nm
Line Width	31.9	0.518
LWR <3σ>	3.12	0.409
Left LER <3σ>	4.326	0.447
Right LER <3σ>	4.074	0.375
Pitch	123.8	0.368

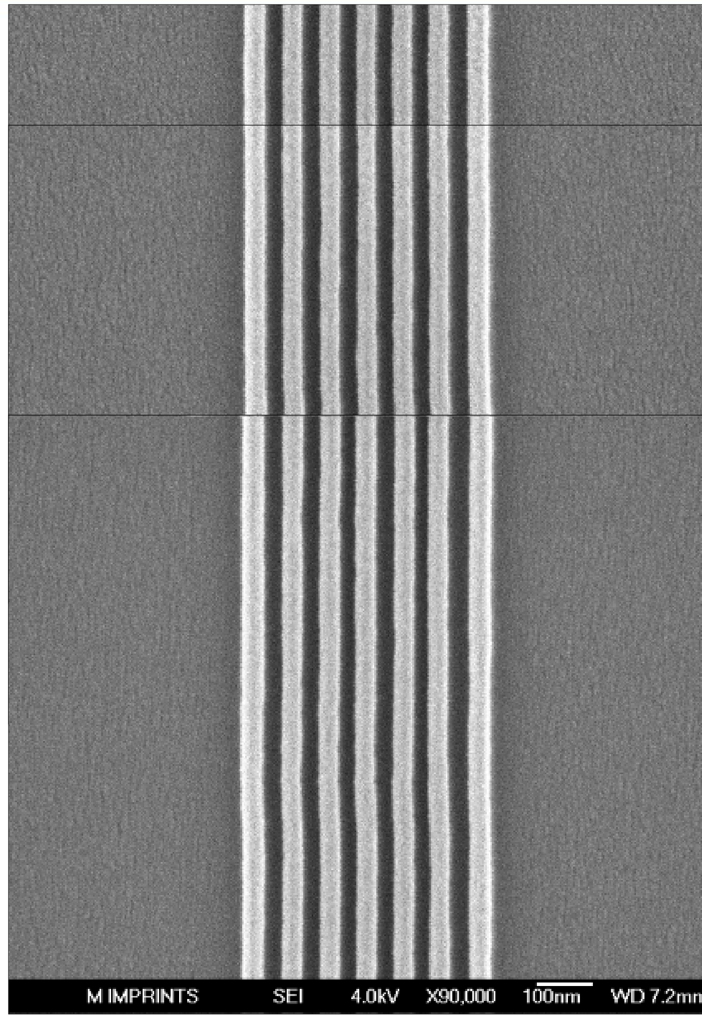


- CD is linear from 32 to 44nm (to within about 5%)
- LWR is small, and independent of critical dimension

32nm Imprint Evaluation



- Imprints #1 and #2 are taken from the same location
- Imprint #3 is located 2mm from Imprint #1



#1
LWR=2.55nm

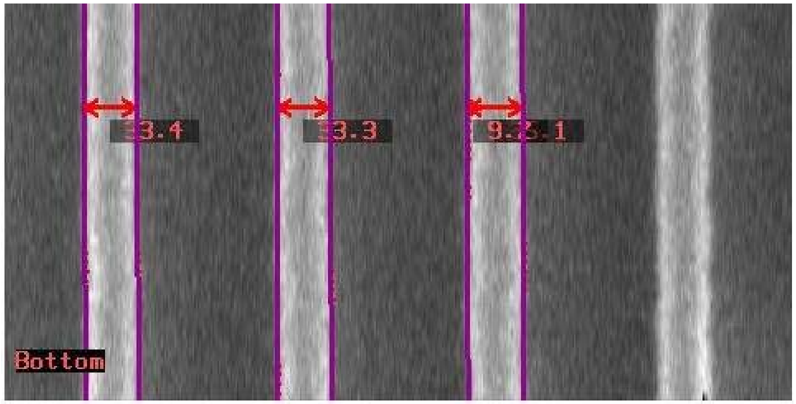
#2
LWR=3.05nm

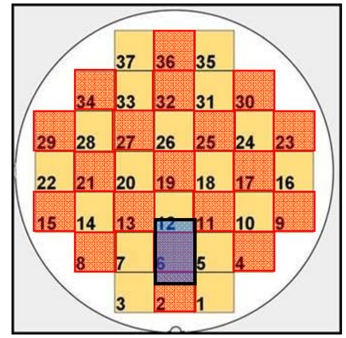
#3
LWR=2.60nm

30 nm and 40 nm design: LWR after etch into SiO_2

atdf

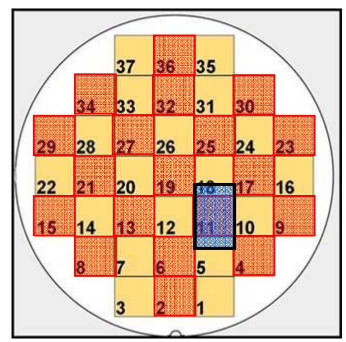
30 nm design
Field 6





LWR (nm, 3σ) = 1.91 | 2.15 | 2.56
LER | | 1.76

40 nm design
Field 11



LWR (nm, 3σ) = 2.05 | 1.79 | 2.40
LER | | 1.01

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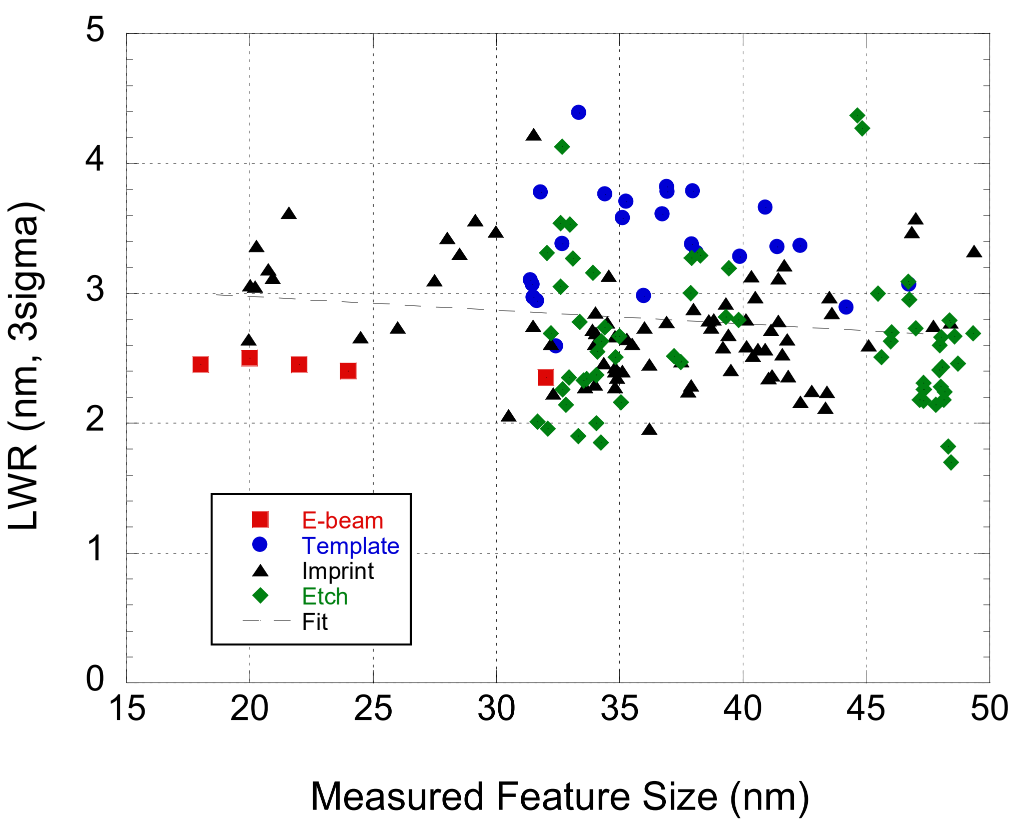
Summary of Line Width Roughness Data



 # lines measured: 170

- LWR_{mean} = 2.79nm
- LWR_{min} = 1.70nm
- LWR_{max} = 4.39nm
- 3σ = 1.59nm

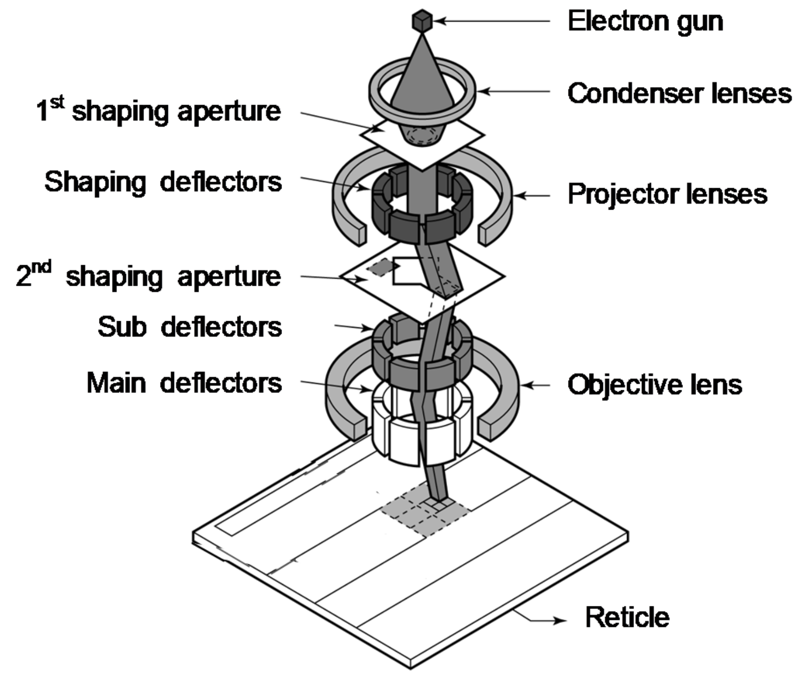
Variable Shape Beam Pattern Generators

Variable Shape Beam PGs (VSBs)

NuFlare EBM 6000 plus

VSB systems are e-beam tools of choice for writing 4x photomasks

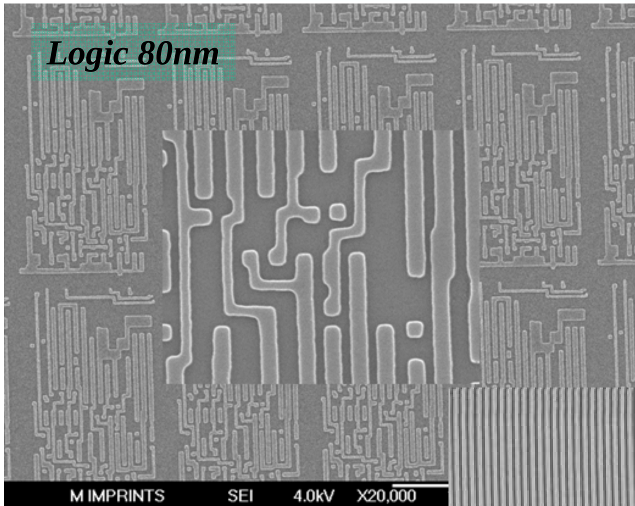
System Architecture



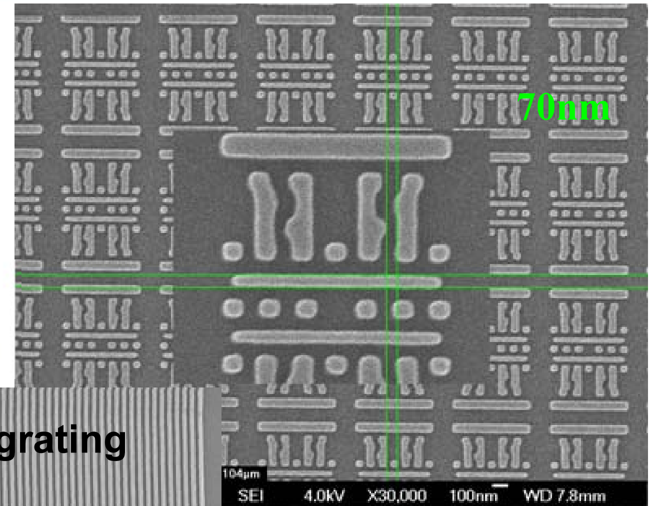
J. Yashima et al, Photomask Japan 2007

Old Wives Tale 9647: VSB tools are the correct choice if you need to write fast, but they don't have great resolution

VSB: Commercial Shops – CA Resists



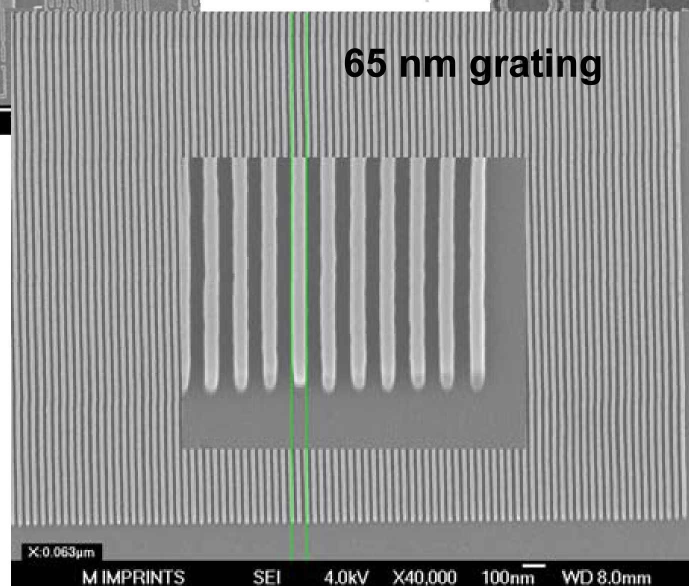
DNP



TOPPAN

TOPPAN PHOTOMASKS, INC.

IMS chips



EIPBN: May 2005

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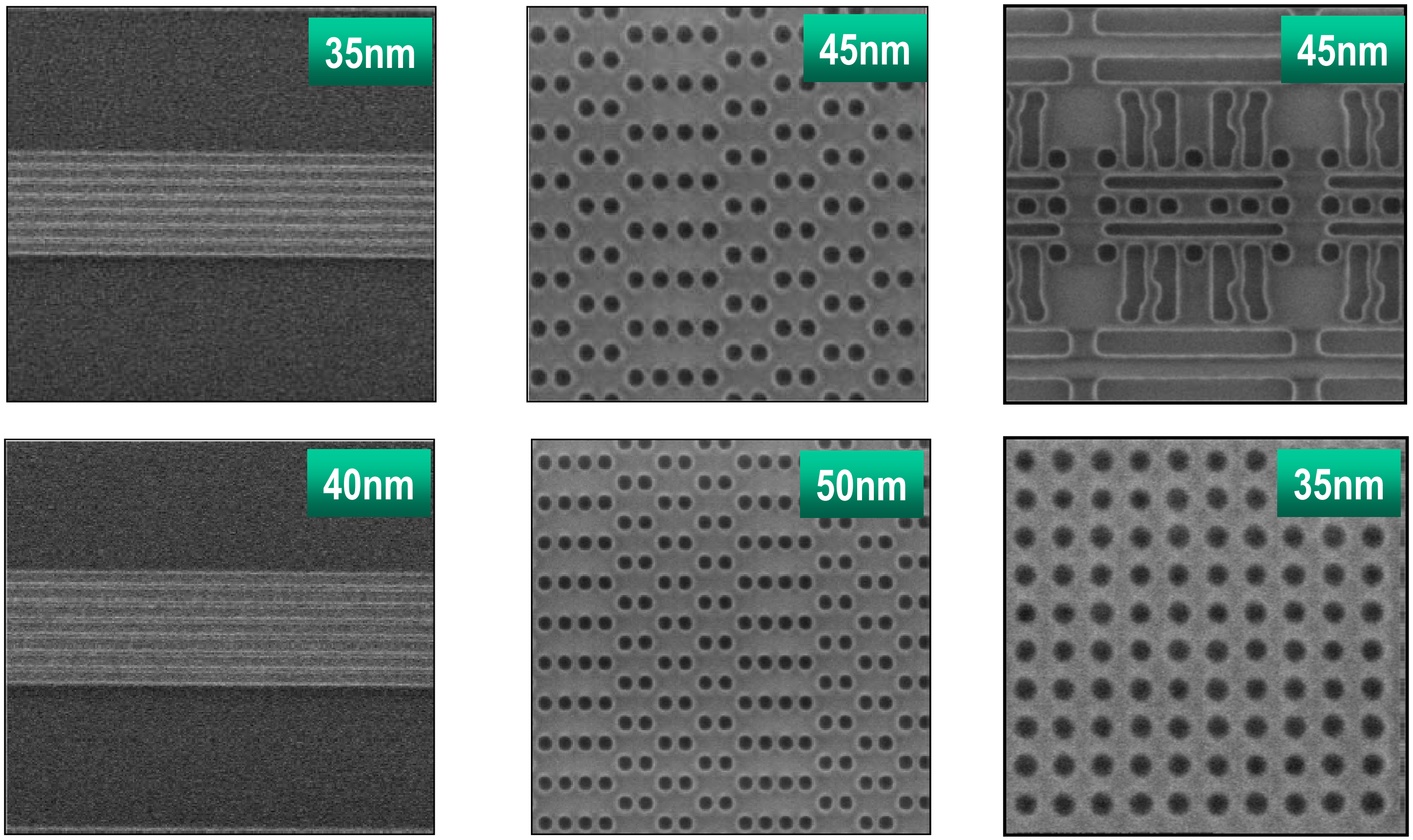
Exposure Results: VSBs and ZEP520A

ZEP520A Resist Images: EBM-5000



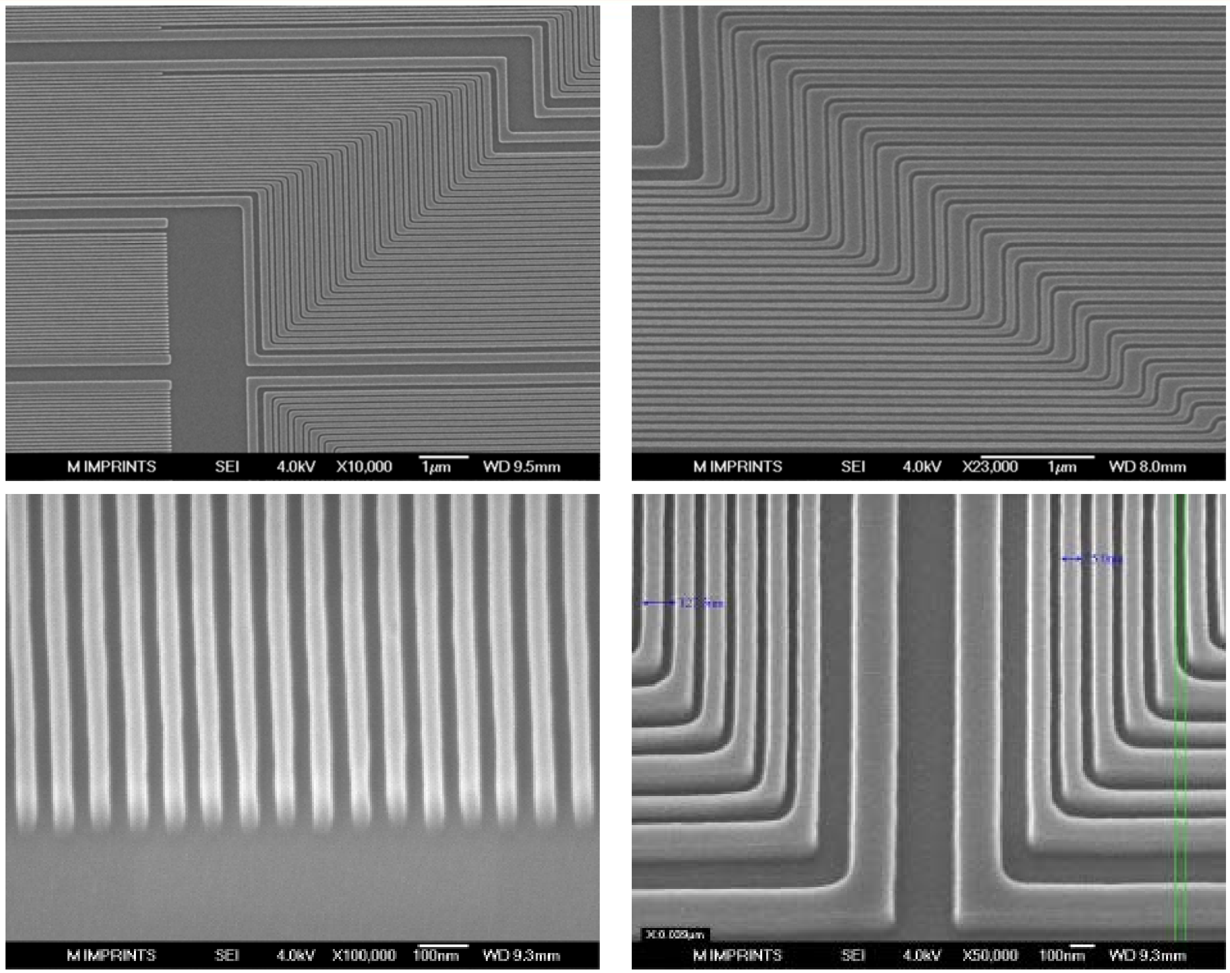
38nm Half Pitch NAND Flash: Gate Level

SAMSUNG

DNP

Resolution & LWR
both excellent

Imprint Results: SPIE: Feb 2008



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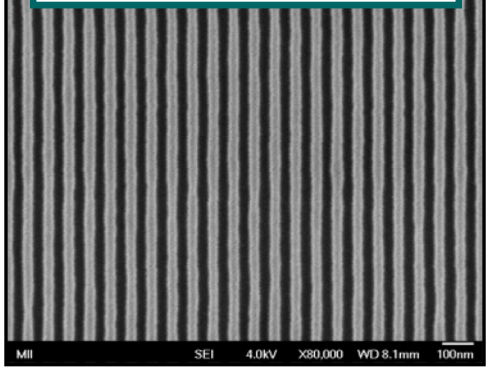
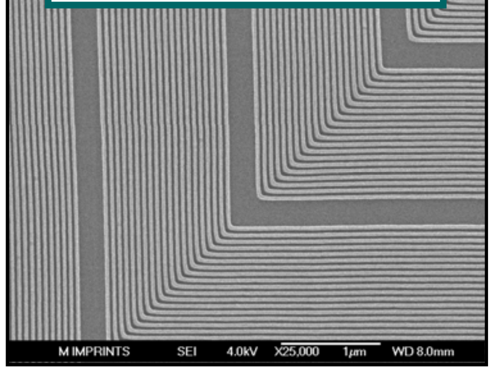
VSB: 32nm Imprints

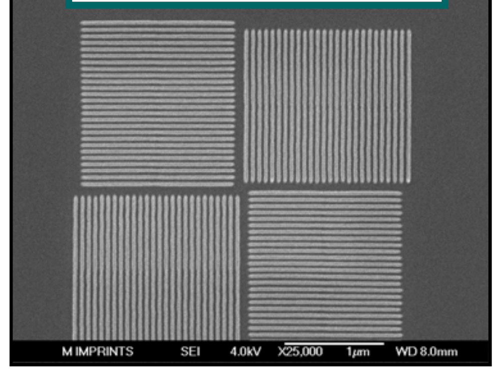
32nm half-pitch



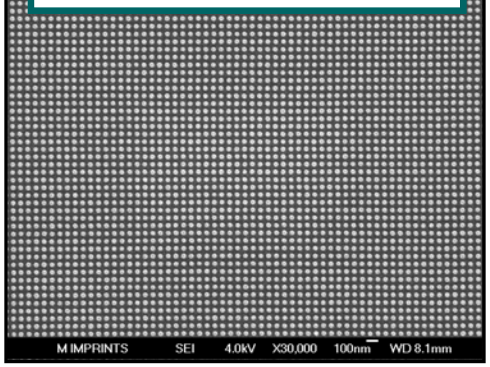
32nm Hor/Vert



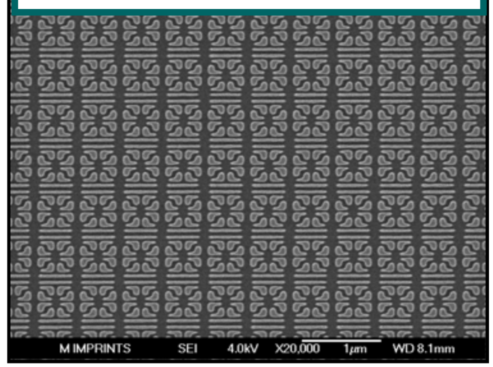
32nm x-hatch



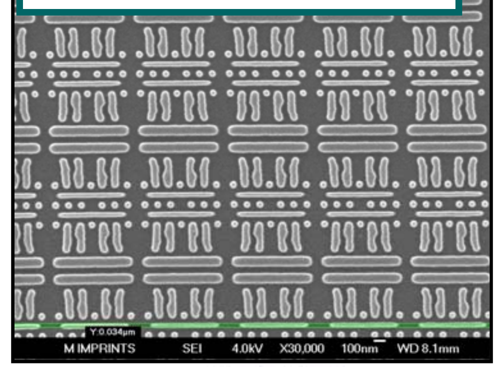
32nm HP Pillars



32nm CMOS Test

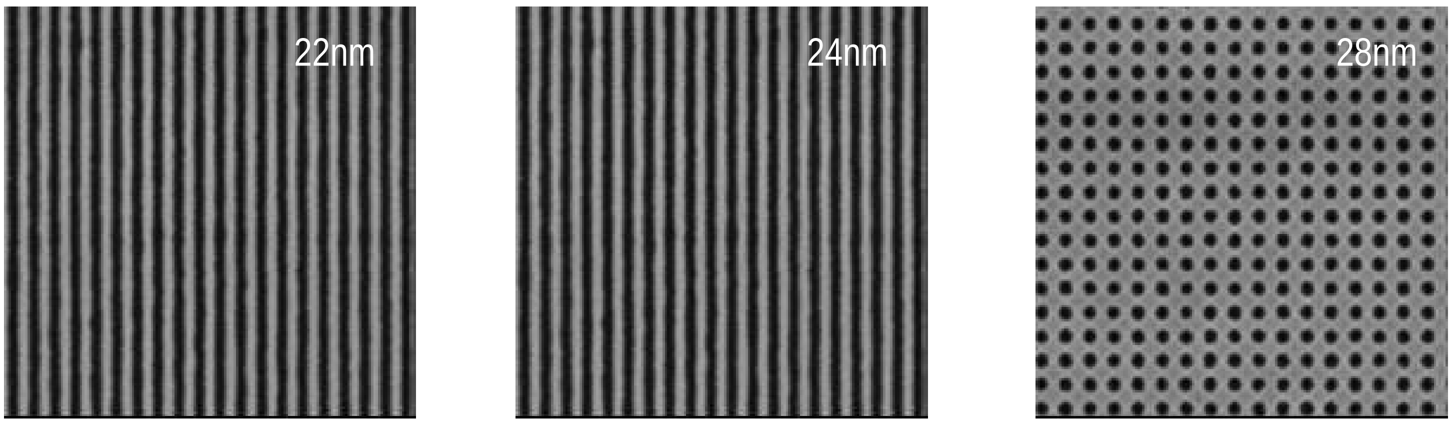


32nm Metal-1

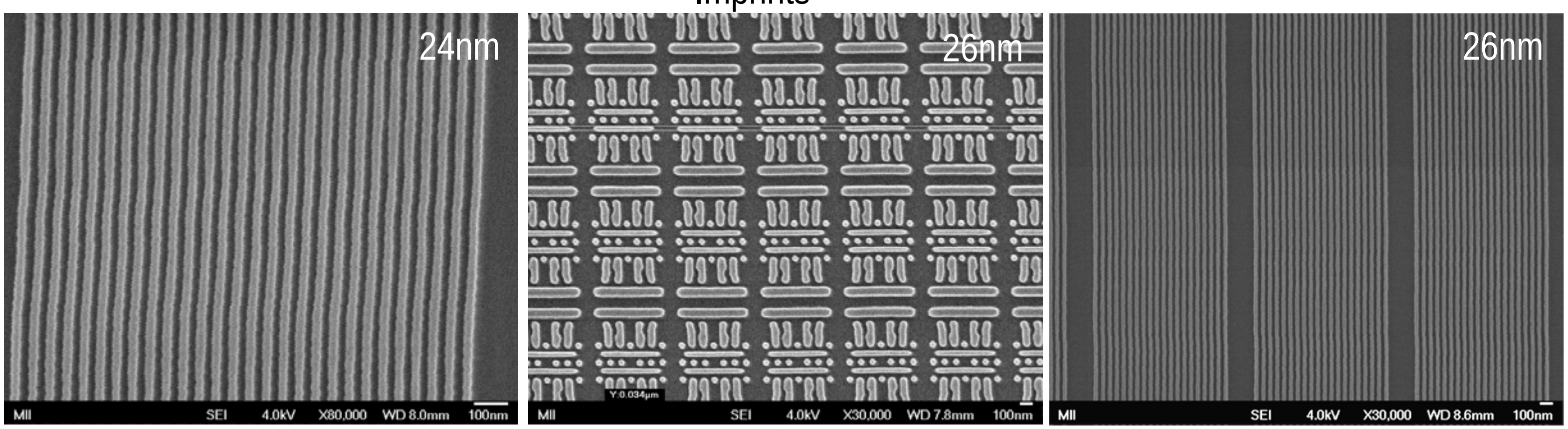


Sub-32nm from VSB PGs

Imprint Mask



Imprints



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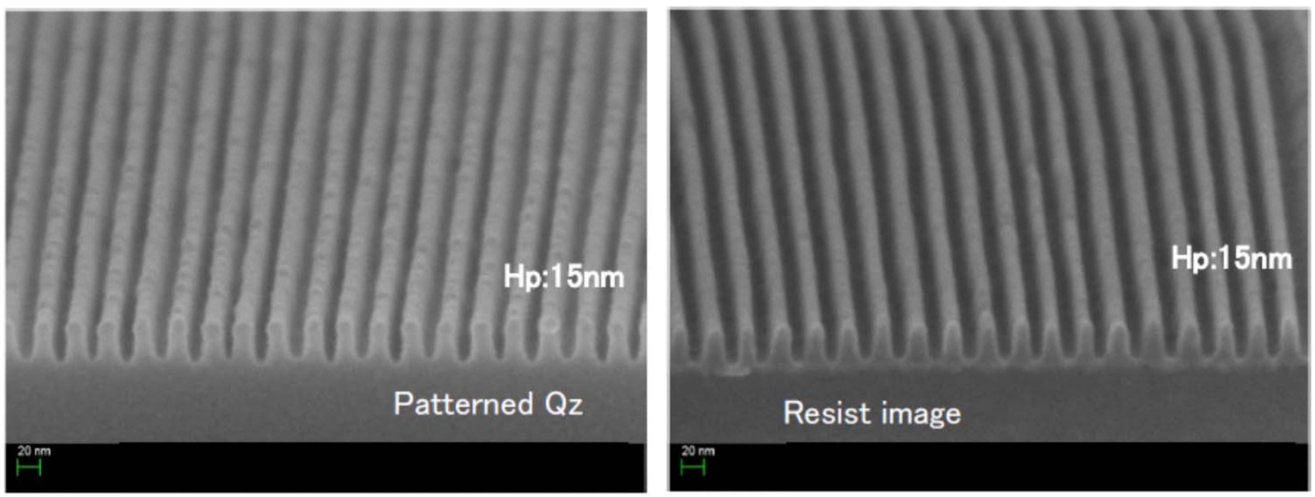
Sub 20nm Masks from VSB PGs

- Current NAND Flash devices are now being fabricated at half pitches of less than 20nm
- How do we make a sub-20nm mask from a VSB tool?

1x imprint demonstation

Master

Imprint



OK, how can they do that?

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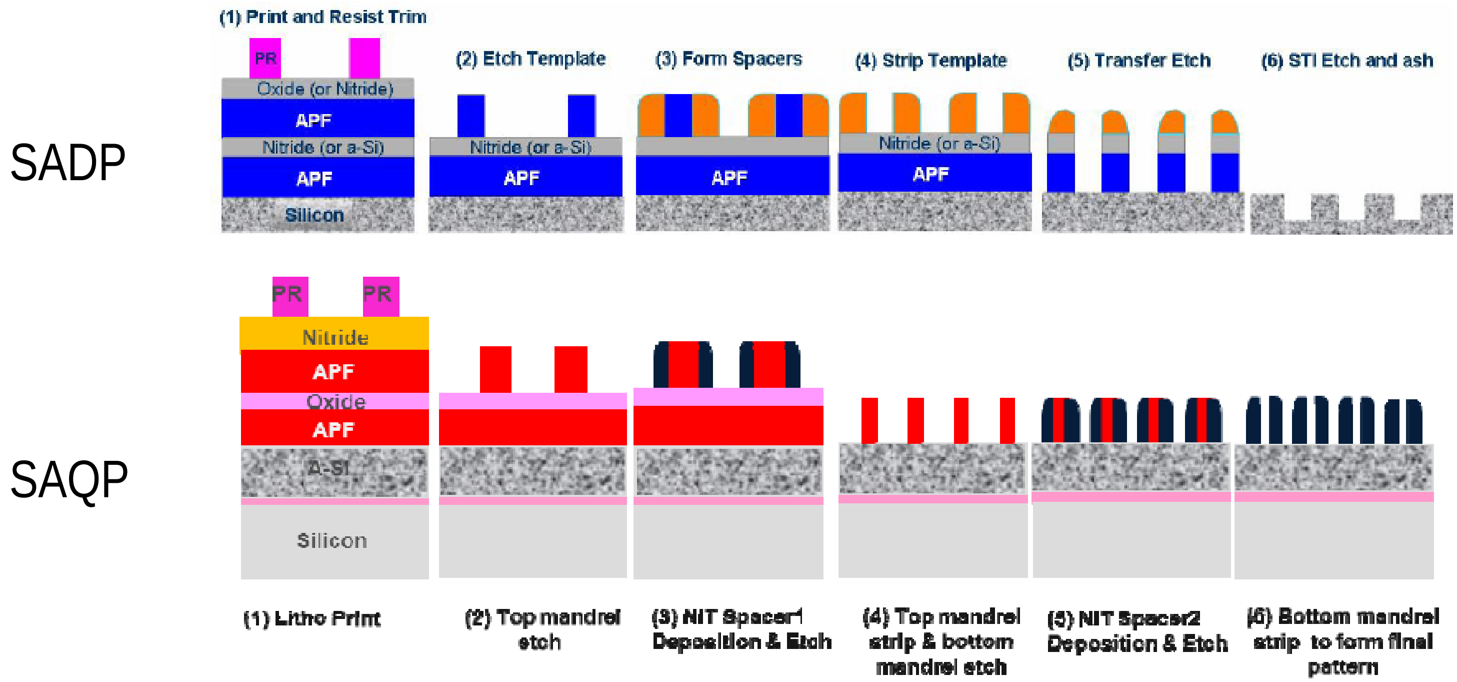
Density Multiplication

- Density multiplication, also referred to as self aligned spacer double patterning is a standard process of record used to make high density NAND Flash devices



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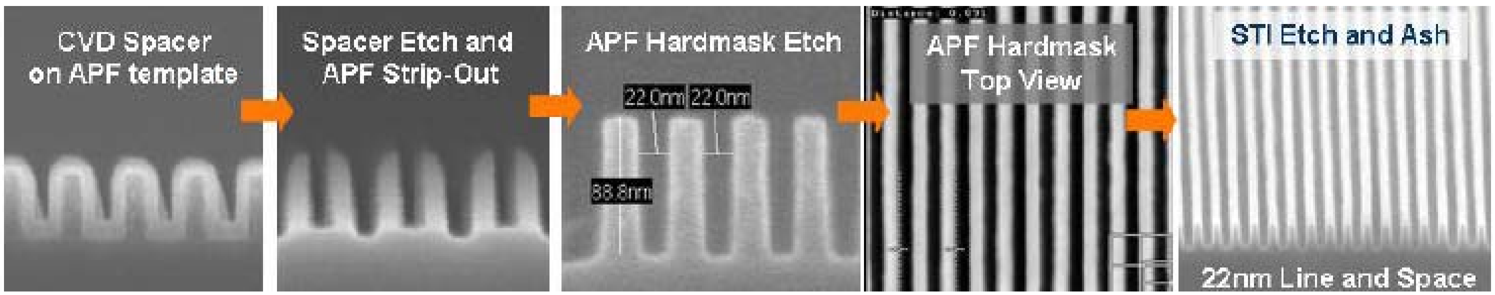
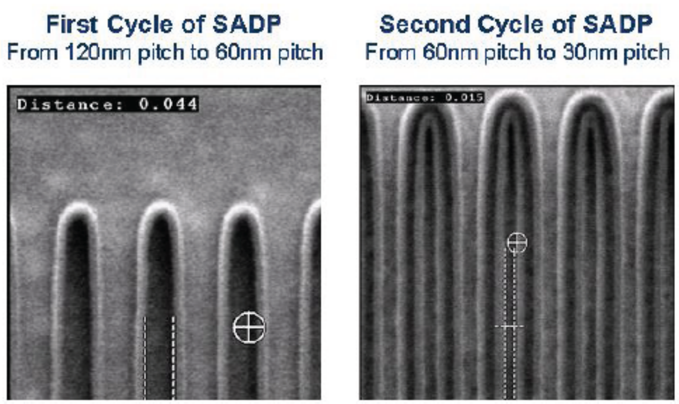
ıprints

Some Density Multiplication Examples

SADP



SAQP



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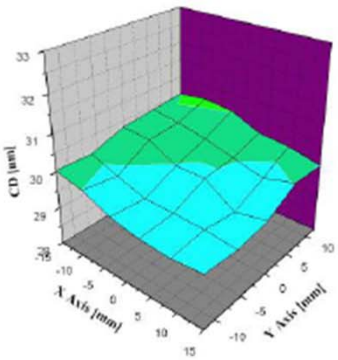
CDU and Image Placement Comparison

CD Uniformity

GB

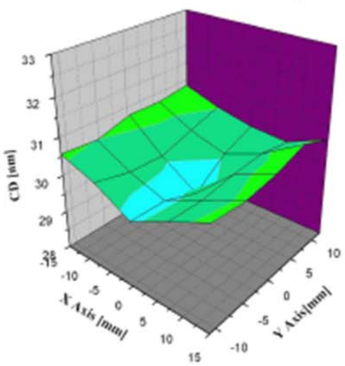
Area 30X24mm (6X5 arrays)



Average : 29.9 nm
Range : 1.3 nm
3σ : 1.2 nm

VSB

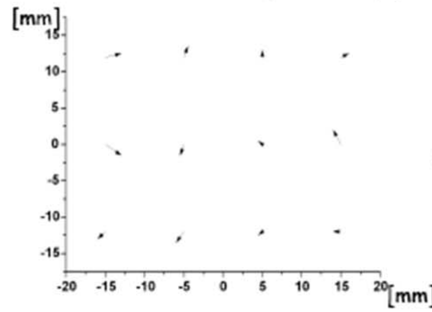
Area 32X26mm (5X5 arrays)



Average : 30.4 nm
Range : 2.1 nm
3σ : 1.7 nm

Image Placement

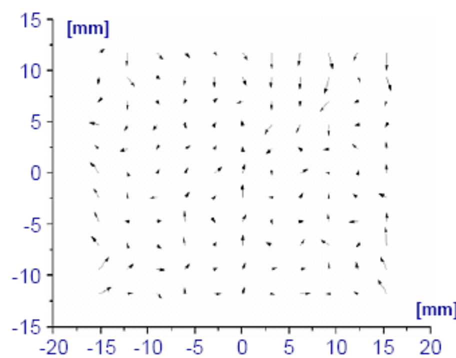
Area 30X24mm (4X3 arrays)



	X	Y
3σ :	6.0 nm	6.0 nm
Min :	-2.0 nm	-3.0 nm
Max :	4.0 nm	4.0 nm

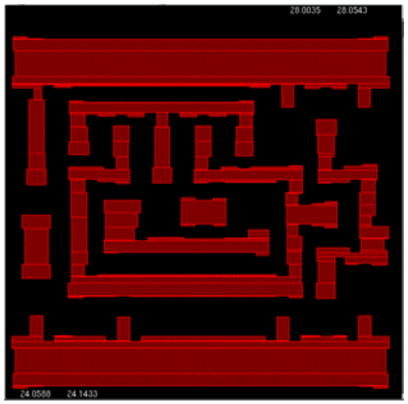
50kV VSB

Area 30 x 26 mm (11 x 11 arrays)



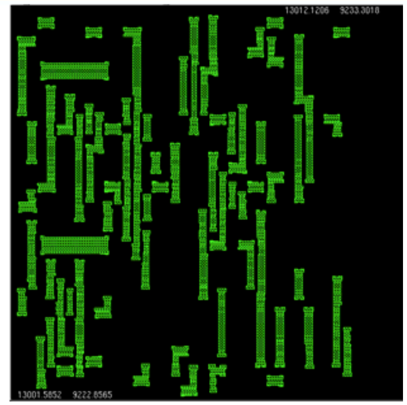
	X	Y
3sigma	2.9	4.2
Min	-2.0	-3.0
Max	2.0	4.0

Write Time Patterns



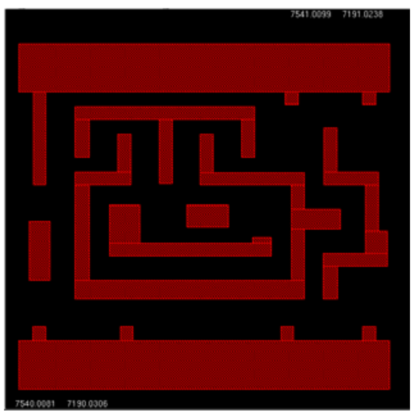
Reticle A
Pattern density:
39.68%

Optical mask A (with OPC)



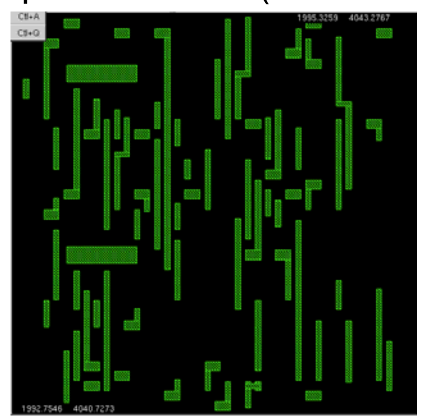
Reticle B
Pattern density:
15.88%

Optical mask B (with OPC)



Template A
Pattern density:
36.68%

Template A (without OPC)



Template B
Pattern density:
11.78%

Template B (without OPC)

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Write Time Results

NuFLARE

Pattern A	Shot counts [G shot]	Writing time [hh:mm:ss]
Template, ZEP520A	223.7	22:51:43
4X Mask, FEP171	385.1	25:49:18
4X Mask, PRL009	770.3	62:24:05

Pattern B	Shot counts [G shot]	Writing time [hh:mm:ss]
Template, ZEP520A	78.6	8:17:29
4X Mask, FEP171	336.5	22:48:37
4X Mask, PRL009	673.0	54:23:02

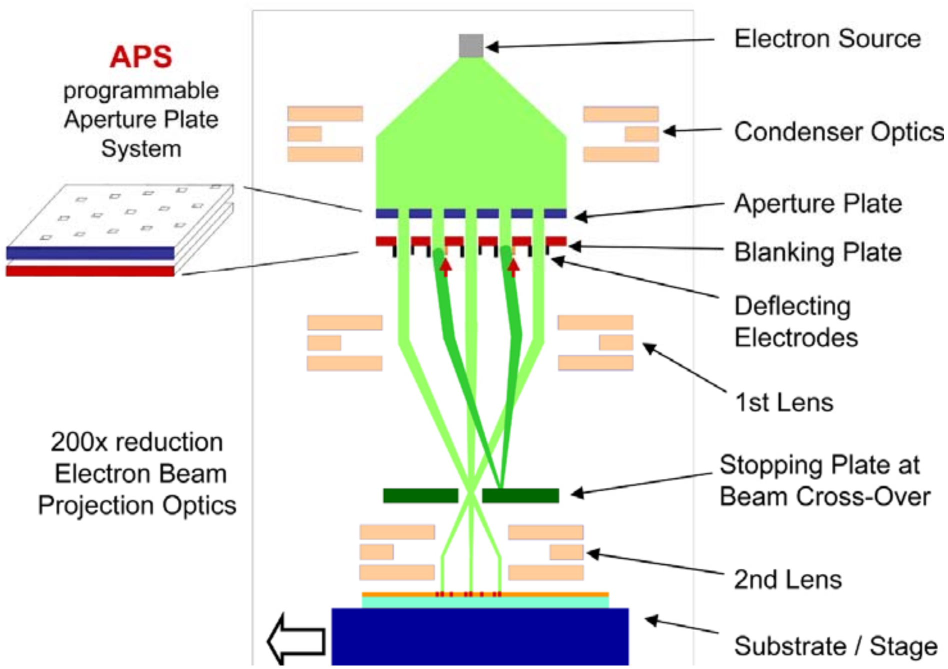
When all is said and done, e-beam machines are slow!

How can we make them write faster?

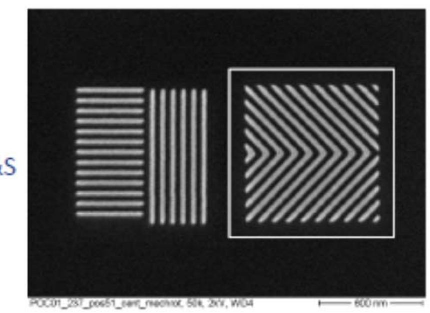
262,000 beams!!!

IMS Nanofabrication

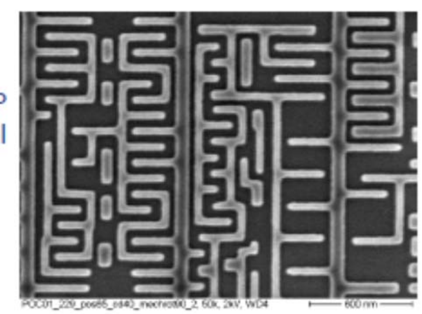
PML2 – Projection Mask-Less Lithography



30nm HP
0°,45°,90° L&S



40nm HP
Metal



Probably good for fast mask writing, but maybe never for wafer writing

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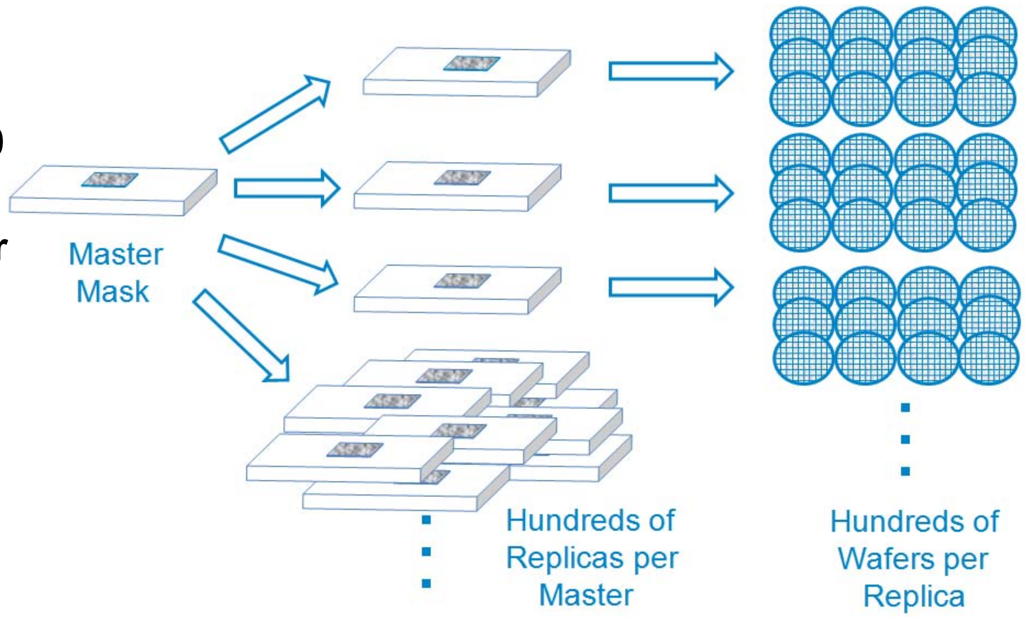
Mask Replication

- The lifetime of a mask is anticipated to be ~ 50,000 – 100,000 imprints
- An e-beam written master mask will cost ~ $500K
- If you wanted to print 1M wafers, you would spend ~ $500M on masks
- Go share that strategy with a fab manager!!!



- The solution: create a Master Template that can easily be replicated
- Master → Daughter approach
- Good news! You can use an imprinter to make the Daughter Templates