Mask Fabrication For Nanoimprint Lithography

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Template (Imprint Mask) Fabrication: Outline

• E-beam and Etch Basics
• Thermal IL Template Fabrication Process
• Templates for Soft Lithography
• J-FIL Templates
  - Processing Challenges
  - Mask Shop Compatible Process
• Commercial Path for Templates
  - Gaussian based templates
    ■ Resolution and Line Width Roughness (LWR)
  - Variable Shape Beam templates
    ■ Resolution, Image Placement, Write Time
  ■ Mask Replication
    ■ Template Inspection
    ■ Template Repair
• Templates for full wafer/disk, and R2R imprinting
• Conclusions

By the end of the course, you will know how to fabricate (or better yet, order) your own templates
First, A Brief History Lesson

EUVL: Started late 1980’s
EPL: Started ~ 1990
MBDW: Started in the 1980’s
193Immersion: Started ~2001

Imprint Lithography
1041 Movable clay type invented in China.
1436 Gutenberg commenced work on his press.
1440 Gutenberg completed his press which used metal moving type.
1455 Gutenberg completed work on his 42 Line Bible.
1455 Gutenberg was effectively bankrupt.
1456 Mazarw Bible printed in Mainz.
1462 The attack on Mainz by soldiers of the Archbishop of Nassau, caused printers to flee and spread their skills around Europe.
1477 The first book to be printed in England (by Caxton)
1499 Printing established in more than 250 cities in Europe.
Mask Basics

• For a photomask, light is projected through the mask, through a lens (with 4x reduction optics) and an aerial image is projected into a photoresist on a silicon wafer

• For an imprint mask (or template), the final resist image depends almost entirely on the relief feature on the template
Template Fabrication

Fabrication of a template generally requires:
- Patterning of a resist (Electron beam writing system)
- Pattern transfer of the pattern into an underlying material (RIE)

**E-beam Systems**

Gaussian-Beam tool

Shaped-Beam Tool

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Electron Beam Writing Strategies

Gaussian Beam

Pros and Cons
• Small spot size
• Dreadfully slow
• Example: Vistec VB300

Shaped Beam

Pros and Cons
• Much faster
• Resolution limited by blur
• Example: NuFlare EBM 7000

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Electron Scattering Basics
(Subtitle: Why electron beam lithographers are unhappy people)

Proximity Correction

\[ M(r) = \frac{1}{\pi(1 + \eta)} \left[ \frac{1}{\alpha^2} \exp\left(-\frac{r^2}{\alpha^2}\right) + \frac{\eta}{\beta^2} \exp\left(-\frac{r^2}{\beta^2}\right) \right] \]

\( \alpha \)-forward scattering coeff.
\( \beta \)-backscattering coeff.
\( \eta \)-ratio of backscattering to forward

Uncorrected
Proximity Corrected

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Etch Basics: Sputtering

- Sputtering has an angular dependence (faceting).
- Sputtering reduces the need for product volatility.
- Sputtering provides directional anisotropy.
- Inert gases provide good yields and avoid contamination.
- Redeposition is an issue.
- Aspect ratio is limited.

<table>
<thead>
<tr>
<th>Ion Energy (eV)</th>
<th>Reaction</th>
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<tbody>
<tr>
<td>&lt;3</td>
<td>Physical absorption</td>
</tr>
<tr>
<td>4 - 10</td>
<td>Surface sputtering</td>
</tr>
<tr>
<td>10 - 5000</td>
<td>Sputtering</td>
</tr>
<tr>
<td>10,000 - 20,000</td>
<td>Implantation</td>
</tr>
</tbody>
</table>

*After Berkeley Labs*
Etch Basics: Chemical Etching

- At higher pressures, substrate removal is accomplished primarily by reactive species generated in the plasma.
- Reaction rate can be strongly influenced by ions
  - damage
  - clean
  - energy for reaction
- Low pressure results in normal ion incidence, but also typically lower ion densities.
  - A variety of tool configurations are available on the market to address specific applications.

*After Berkeley Labs

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The most common IL template is simply a patterned silicon wafer.

- Template
- Silicon thermoplastic
- Thermoset
- Substrate

- E-beam pattern resist
- Etch silicon
- Strip Resist

Silicon can be etched with $SF_6$, $CF_4$, $Cl_2$, $HBr$, etc...

S. Chou, Princeton

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Silicon Etch

- Cl₂ and HBr chemistries tend to etch silicon more anisotropically

- SF₆ and CF₄/O₂ tend to undercut the feature (end product is SiF₄)

- Resist alone is not always a sufficient etch mask. Oxides, nitrides, and chrome are often used as hard masks
Another popular IL template scheme uses SiO$_2$ as the mold.

**Ion enhanced reaction, selective to Si**

* Plasma Etching: Daniel Flamm

10 nm SiO$_2$ pillars on silicon

*from Chou
Soft Lithography Templates

Polydimethylsiloxane (PDMS)

Elastomeric material: polymer chain of silicon containing oils

\[
\begin{align*}
&\text{CH}_3 - \text{Si} - \text{O} - \text{Si} - \text{O} - \text{Si} - \text{CH}_3 \\
&\text{CH}_3 - \text{Si} - \text{O} - \text{Si} - \text{O} - \text{Si} - \text{CH}_3 \\
&\text{CH}_3 - \text{Si} - \text{O} - \text{Si} - \text{O} - \text{Si} - \text{CH}_3 \\
&\text{CH}_3 - \text{Si} - \text{O} - \text{Si} - \text{O} - \text{Si} - \text{CH}_3 \\
&\text{CH}_3 - \text{Si} - \text{O} - \text{Si} - \text{O} - \text{Si} - \text{CH}_3 \\
\end{align*}
\]

Example: Sylgard 184: Dow Corning

Tensile strength: 7.1 MPa
Elongation at break: 140%
Tear strength: 2.6 kN/m
PDMS Fabrication Process

- Master
- Liquid Precursor to PDMS
- PDMS Stamp
- Master Features
- Microfluidic device
- FET

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J-FIL Template Layout for Semiconductors

6” x 6” x 0.25” (6025) quartz blank substrate
Patterned area rests on a mesa (15-30um)

26mm x 33mm Patterned area

Thick resist over 15 nm Cr
15 μm high pedestal
J-FIL Template Attributes

Template Attributes:

- Transparent to UV light
- Compatible with a release layer
- Compatible with alignment schemes
- Mechanically durable
- Chemically durable (cleaning)
- Manufacturable
  - Good CD control
  - Good Image Placement
  - Low Defectivity
  - Inspectable: UV, DUV, e-beam
  - Repairable

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Conventional Photomask Processing

To fabricate a J-FIL Template, we need to add one more step

This process is currently used in mask shops to fabricate phase shift masks

So, What’s the Problem?
• We’re making 1X masks, so we must dry etch
• Dry etching of Cr is subject to undercut and loading effects

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Chromium Etching

\[ \text{Cr} + 2\text{O}^* + 2\text{Cl}^* \rightarrow \text{CrO}_2\text{Cl}_2 \]

**Issues:**

- The etch has a large chemical component: undercut
- The process requires a lot of oxygen (25%): resist loss
- The process is subject to loading effects: CD variation
J-FIL Template Fabrication Schemes

To minimize these effects, reduce the Cr thickness

- Resist applied to <15 nm of Cr
- Expose/develop e-beam resist, descum
- Etch chrome, strip resist
- Etch quartz, Strip chrome

- Compatible with existing Mask Shop Processes
  - Leica VB6 operating at 100 kV
  - 5 nm address grid
  - ZEP520 positive e-beam resist
  - Track processing on an EVG 150/160
  - Etching: Unaxis VLR
  - Gas Chemistry: Cr – Cl₂/O₂, SiO₂ – CF₄/O₂

Following Slides:
ZEP520 Exposure/Descum

ZEP520A process latitude is excellent

2.6nm change for every 20 seconds

Final CD Bias (nm)

Exposure Dose (μC/cm²)

Descum Time (s)
Cr Process CD Results

- All results shown are for 80 nm features.
- Similar to observations made for increasing descum time, a positive CD change of 3.8 nm per 20% of Cr overetch exists.

![Graph showing final CD bias vs. chrome overetch (%)]

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FIB/TEM Feature Profile

- Cross-sectioning the trenches was done using a focused ion beam tool in conjunction with a protective film stack to avoid extreme charging, sample drift, and surface damage.

- Using TEM measurements as a basis, sidewall angles of 150 nm features were calculated to be ~ 84°

- The measured etch depth of 98 nm compares extremely well to profilometer and AFM measurements.

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Fabrication Window

- A 20 s descum coupled with a 110% Cr overetch was found to give the best performance in terms of CD control and line edge roughness.

- For 60 nm clustered features, the spaces measure ~ 4 nm over coded size.
- The descum process increases CD by about the same magnitude.
- Resist erosion during Cr etch results in approximately 7 more nanometers of bias.
- After quartz etch, CD bias is 1.5 nm less than coded. The quartz sidewall angle is about 5° from the normal.
- Final CD bias ends up approximately 1 nm from coded after the Cr hardmask is stripped.
Pattern/Pattern Transfer Process

<table>
<thead>
<tr>
<th>60 nm</th>
<th>40 nm</th>
<th>30 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resist</td>
<td>Descum</td>
<td>Cr Etch</td>
</tr>
</tbody>
</table>

SPIE: Feb 2002
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Pattern Transfer Process

HP32nm  HP28nm  HP24nm  HP20nm

Resist
Chrome
Quartz

PMJ: April 2008

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Magnification: 150k
Resolution with 100kV GB writer

Line & Space pattern  1/2Pitch

Etched quartz images

Nanoimprint & Nanoprint Technology 2009
Electron Beam Pattern Generators

There are two methods for generating patterns on a template:

1. **Gaussian beam PGs**: Great for unit process development and device prototyping

2. **Variable Shaped Beam PGs**: Needed for full field pattern generation and for image placement

- How do I get the best result from each tool?
  - Resolution
  - Line Width Roughness
  - CD uniformity
  - Image Placement
  - Write Time
Gaussian Beam Pattern Generators
ZEP520A Process Development

- Resist response was studied for a variety of different developers
  - Amyl Acetate developer provides a good combination of contrast and sensitivity
  - Numbers next to curves indicate the digitized CD

- Exposure latitude of the resist was mapped as a function of feature bias
  - Exposure latitude is improves as biasing of critical features increases
  - Xylenes, o-Xylene, Amyl acetate, Hexyl acetate
  - 80 nm pitch grating
Development of ZEP520A resist

- Sonication of developer bath
- Dilution of developer
  - Equal mixture of amyl acetate with isopropyl alcohol
  - 120 s puddle development
  - 60 s isopropyl alcohol rinse, dry

![22 nm half-pitch](image1)
![18 nm half-pitch](image2)

Graph showing CD normalized dose (µC/cm²) vs. CD (nm) with negative bias of 12 nm.
Imprint Resolution

- 28nm half-pitch
- 25nm Contacts
- 22nm half-pitch

- 22nm Fan-out
- 20nm Half Pitch
- 20nm Half Pitch
Line Width Roughness (LWR)

- Variation in CD along the length of a line
  - Results in variation of MOS gate width
  - Affects device speed of individual transistors
  - Leads to IC timing issues

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<tbody>
<tr>
<td>LWR</td>
<td>3.4</td>
<td>2.4</td>
<td>1.7</td>
<td>1.2</td>
<td>0.8</td>
</tr>
</tbody>
</table>

ITRS Roadmap for LWR (nm, 3σ)

Future nodes have no known solutions.

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LWR Example: EUVL

Throughput requirements of EUVL require the use of fast chemically amplified resists
- Low exposure doses required for throughput
  - Too few photons: \( \sim 2 / \text{nm}^2 \)
  - Shot noise effects

RLS Trade-Off for Chemically Amplified Resists
Resolution vs. LWR vs. Sensitivity
(Robert Brainard, Gregg Gallatin)

So, is imprint lithography immune to this problem?
YES! And NO!!

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Pattern formation with J-FIL technology

**Imprint Mask Fabrication**

**Resolution and LWR**

- Use non-CA resists for best resolution and LWR performance.
- Utilize existing photomask infrastructure for fabrication and inspection.

**Imprint Patterning**

**Throughput**

- CD, CDU, LWR, etc. of the patterned resist is determined by the template.
LWR minimization at 22 nm

Parameter mean

- Line Width, nm: 23.36 ± 1.28
- LWR <3σ>, nm: 2.15 ± 0.29

Gaussian E-Beam exposure at 100kV

250 μC/cm²: ~15 electrons / nm²

LWR = 2.45 nm, 3σ

22 nm HP

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Template: CD and LWR Analysis

- CD is linear from 32 to 44nm (to within about 5%)
- LWR is small, and independent of critical dimension

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Mean, nm</th>
<th>Std. dev., nm</th>
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</thead>
<tbody>
<tr>
<td>Line Width</td>
<td>31.9</td>
<td>0.518</td>
</tr>
<tr>
<td>LWR &lt;3σ&gt;</td>
<td>3.12</td>
<td>0.409</td>
</tr>
<tr>
<td>Left LER &lt;3σ&gt;</td>
<td>4.326</td>
<td>0.447</td>
</tr>
<tr>
<td>Right LER &lt;3σ&gt;</td>
<td>4.074</td>
<td>0.375</td>
</tr>
<tr>
<td>Pitch</td>
<td>123.8</td>
<td>0.368</td>
</tr>
</tbody>
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32nm Imprint Evaluation

- Imprints #1 and #2 are taken from the same location
- Imprint #3 is located 2mm from Imprint #1

Template: LWR = 3.1nm

#1
LWR = 2.55nm

#2
LWR = 3.05nm

#3
LWR = 2.60nm
30 nm and 40 nm design: LWR after etch into SiO$_2$

**30 nm design**  
Field 6  
LWR (nm, 3$\sigma$) = 1.91  
LER = 2.15  
LER = 2.56  
LER = 1.76

**40 nm design**  
Field 11  
LWR (nm, 3$\sigma$) = 2.05  
LER = 1.79  
LER = 2.40  
LER = 1.01
Summary of Line Width Roughness Data

- \( \text{LWR}_{\text{mean}} = 2.79 \text{nm} \)
- \( \text{LWR}_{\text{min}} = 1.70 \text{nm} \)
- \( \text{LWR}_{\text{max}} = 4.39 \text{nm} \)
- \( 3\sigma = 1.59 \text{nm} \)

# lines measured: 170
Variable Shape Beam Pattern Generators
Variable Shape Beam PGs (VSBs)

VSB systems are e-beam tools of choice for writing 4x photomasks

Old Wives Tale 9647: VSB tools are the correct choice if you need to write fast, but they don’t have great resolution

J. Yashima et al, Photomask Japan 2007
VSB: Commercial Shops – CA Resists

Logic 80nm

65 nm grating

EIPBN: May 2005

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Exposure Results: VSBs and ZEP520A

ZEP520A Resist Images: EBM-5000

BACUS: September 2007

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38nm Half Pitch NAND Flash: Gate Level

Resolution & LWR both excellent

Imprint Results:
SPIE: Feb 2008
VSB: 32nm Imprints

32nm half-pitch

32nm Hor/Vert

32nm x-hatch

32nm HP Pillars

32nm CMOS Test

32nm Metal-1

August 2008

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Sub-32nm from VSB PGs

Imprint Mask

22nm

24nm

28nm

Imprints

24nm

26nm

28nm

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Sub 20nm Masks from VSB PGs

- Current NAND Flash devices are now being fabricated at half pitches of less than 20nm
- How do we make a sub-20nm mask from a VSB tool?

1x imprint demonstration

Master

Imprint

HP: 15nm

Patterned Qz

Resist image

OK, how can they do that?
Density Multiplication

- Density multiplication, also referred to as self aligned spacer double patterning, is a standard process of record used to make high density NAND Flash devices.
Some Density Multiplication Examples

**SADP**

- CVD Spacer on APF template
- Spacer Etch and APF Strip-Out
- APF Hardmask Etch
- APF Hardmask Top View
- STI Etch and Ash

**SAQP**

- First Cycle of SADP: From 120nm pitch to 60nm pitch
- Second Cycle of SADP: From 60nm pitch to 30nm pitch
CDU and Image Placement Comparison

**CD Uniformity**

For GB:
- Area: 30x24 mm (6x5 arrays)
- Average: 29.9 nm
- Range: 1.3 nm
- 3σ: 1.2 nm

For VSB:
- Area: 32x26 mm (5x5 arrays)
- Average: 30.4 nm
- Range: 2.1 nm
- 3σ: 1.7 nm

**Image Placement**

For GB:
- Area: 30x24 mm (4x3 arrays)
- 3σ: 6.0 nm, 6.0 nm
- Minimum: -2.0 nm, -3.0 nm
- Maximum: 4.0 nm, 4.0 nm

For 50kV VSB:
- Area: 30 x 26 mm (11 x 11 arrays)

<table>
<thead>
<tr>
<th></th>
<th>X</th>
<th>Y</th>
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<tbody>
<tr>
<td>3σ</td>
<td>2.9</td>
<td>4.2</td>
</tr>
<tr>
<td>Minimum</td>
<td>-2.0</td>
<td>-3.0</td>
</tr>
<tr>
<td>Maximum</td>
<td>2.0</td>
<td>4.0</td>
</tr>
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Write Time Patterns

Reticle A
Pattern density: 39.68%

Optical mask A (with OPC)

Template A
Pattern density: 36.68%

Template A (without OPC)

Reticle B
Pattern density: 15.88%

Optical mask B (with OPC)

Template B
Pattern density: 11.78%

Template B (without OPC)

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## Write Time Results

<table>
<thead>
<tr>
<th>Pattern A</th>
<th>Shot counts [G shot]</th>
<th>Writing time [hh:mm:ss]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Template, ZEP520A</td>
<td>223.7</td>
<td>22:51:43</td>
</tr>
<tr>
<td>4X Mask, FEP171</td>
<td>385.1</td>
<td>25:49:18</td>
</tr>
<tr>
<td>4X Mask, PRL009</td>
<td>770.3</td>
<td>62:24:05</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pattern B</th>
<th>Shot counts [G shot]</th>
<th>Writing time [hh:mm:ss]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Template, ZEP520A</td>
<td>78.6</td>
<td>8:17:29</td>
</tr>
<tr>
<td>4X Mask, FEP171</td>
<td>336.5</td>
<td>22:48:37</td>
</tr>
<tr>
<td>4X Mask, PRL009</td>
<td>673.0</td>
<td>54:23:02</td>
</tr>
</tbody>
</table>
When all is said and done, e-beam machines are slow!

How can we make them write faster?

262,000 beams!!!

PML2 — Projection Mask-Less Lithography

APS
programmable Aperture Plate System

Electron Source
Condenser Optics
Aperture Plate
Blanking Plate
Deflecting Electrodes
1st Lens
Stopping Plate at Beam Cross-Over
2nd Lens
Substrate / Stage

Probably good for fast mask writing, but maybe never for wafer writing

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Mask Replication

- The lifetime of a mask is anticipated to be ~ 50,000 – 100,000 imprints
- An e-beam written master mask will cost ~ $500K
- If you wanted to print 1M wafers, you would spend ~ $500M on masks
- Go share that strategy with a fab manager!!!

- The solution: create a Master Template that can easily be replicated
- Master → Daughter approach
- Good news! You can use an imprinter to make the Daughter Templates