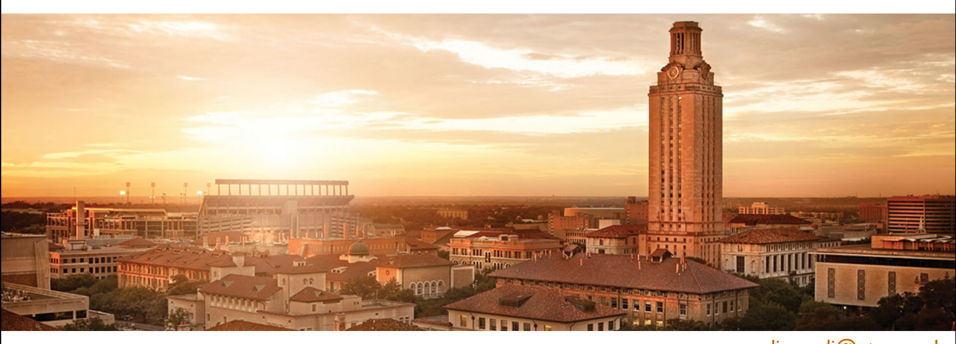
Double Patterning

Rasha El-Jaroudi
November 7th 2017



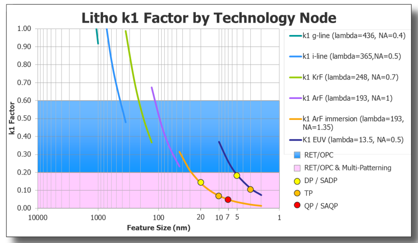
reljaroudi@utexas.edu

Outline

- **Motivation**
- Techniques
- Future of Double Patterning

Motivation

- Need to keep up with Moore's Law
- EUV not ready yet
- Reduce minimum pitch size using existing technology (193nm Immersion Lithography), but have already minimized λ and maximized NA

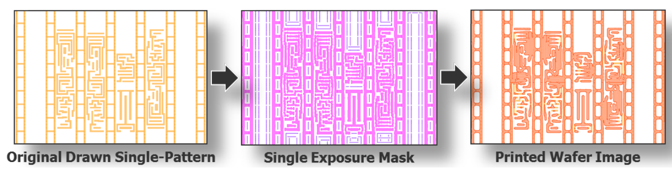


$$R = \frac{k_1 \lambda}{NA}$$

D. Abercrombie, *"Will EUV Kill Multi-Patterning,"* SC Engineering (2017).

Minimizing k_1

- k_1 is defined by process features
- OPC and RET were employed to correct for lithography imperfections
- If k_1 is below 0.2, RET/OPC begins to cause overlaps in neighboring shapes



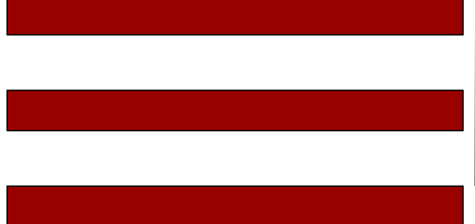
$$R = \frac{k_1 \lambda}{NA}$$

D. Abercrombie, *"Will EUV Kill Multi-Patterning,"* SC Engineering (2017).

Minimizing k_1

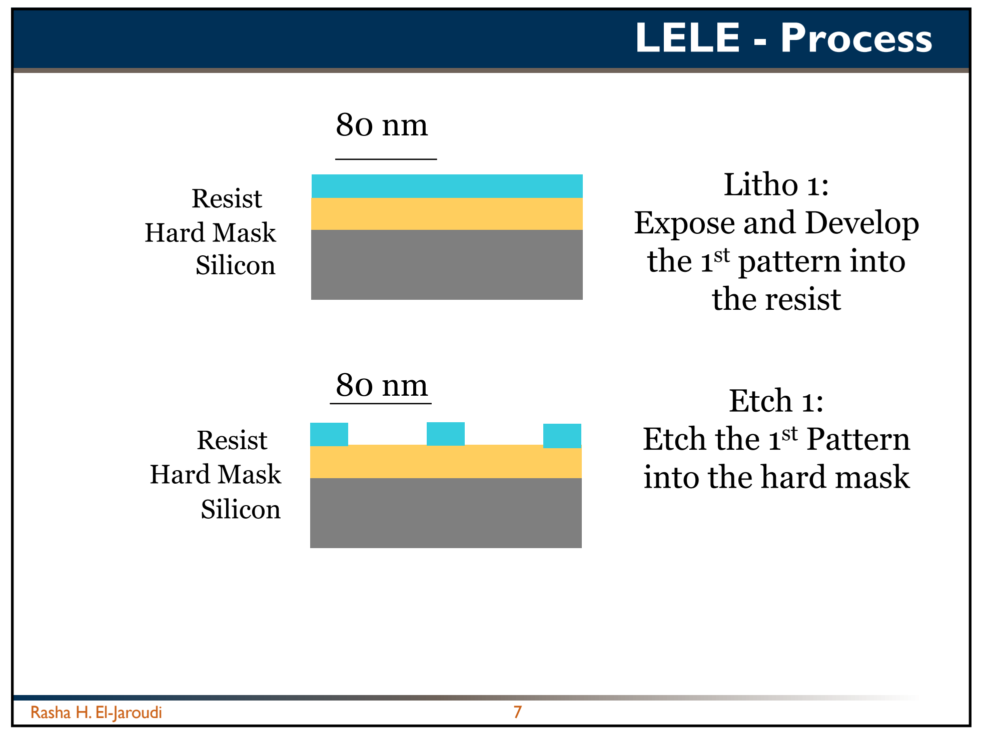
- Lowest half-pitch possible with immersion lithography was 36nm (k=0.25, NA=1.35, and λ=193nm)
- Double patterning can further reduce pitch size without changing NA or λ.

$$R = \frac{0.25 \cdot 193}{1.35} \approx 36\ nm$$



Outline

- Motivation
- **Techniques**
  - Litho-Etch-Litho-Etch (LELE)
  - Self-Aligned Double Patterning (SADP)
  - Litho-Freeze-Litho-Etch (LFLE)
- Future of Double Patterning


LELE - Process
80 nm
Resist
Hard Mask
Silicon
Litho 1:
Expose and Develop the 1st pattern into the resist
80 nm
Resist
Hard Mask
Silicon
Etch 1:
Etch the 1st Pattern into the hard mask
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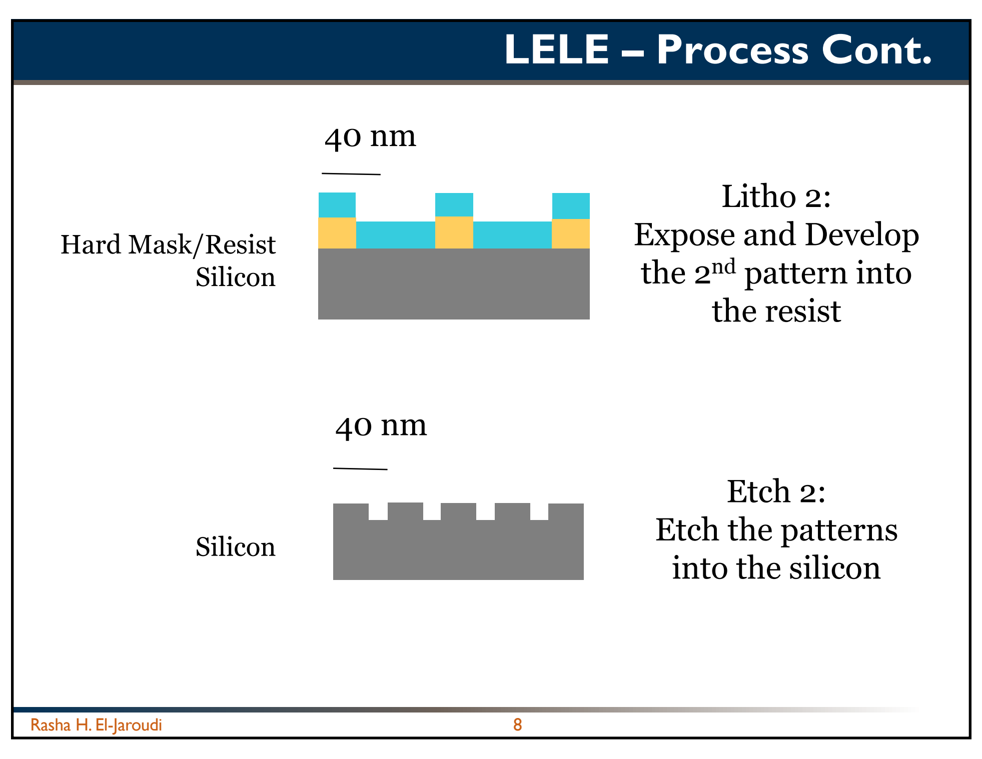
LELE – Process Cont.
40 nm
Hard Mask/Resist
Silicon
Litho 2:
Expose and Develop the 2nd pattern into the resist
40 nm
Silicon
Etch 2:
Etch the patterns into the silicon
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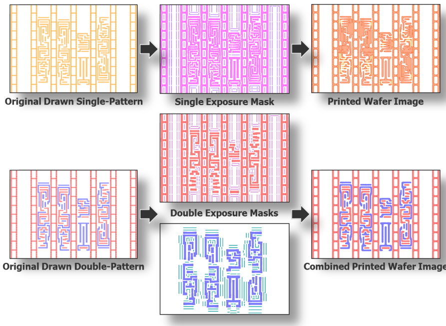
LELE - Advantages

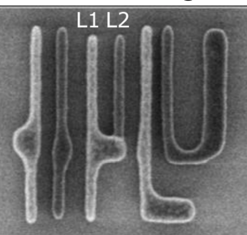
- Advantages
  - No new technology
  - Successfully reduce pitch



D. Abercrombie, *"Will EUV Kill Multi-Patterning,"* SC Engineering (2017).

LELE- Challenges

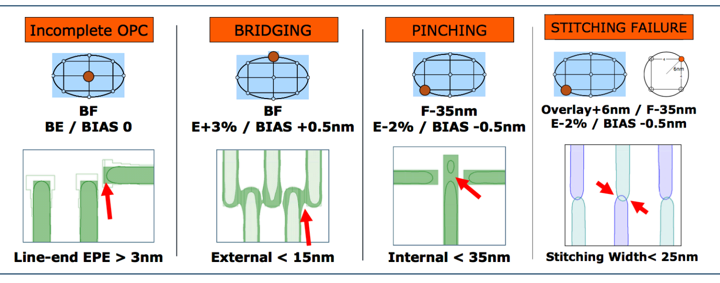
- Twice as many steps as single exposure
  - Increased cost
  - Decreased throughput
- Complicated etch steps
  - First etch step transfers pattern to hard mask
  - Second etch step needs to account for resist and hard mask
- Mask alignment
  - Need to recombine two images to form the intended image



M. Maenhoudt et al. Proc of SPIE Vol. 6924, 692409, (2008)

LELE- Challenges Cont.

- Double patterning is more sensitive to variations in process
- OPC can design for ideal process conditions
- Errors in dose, focus, or mask overlay will affect potential yield



V. Wiaux et al. Proc. of SPIE Vol. 6924, 692409, (2008)

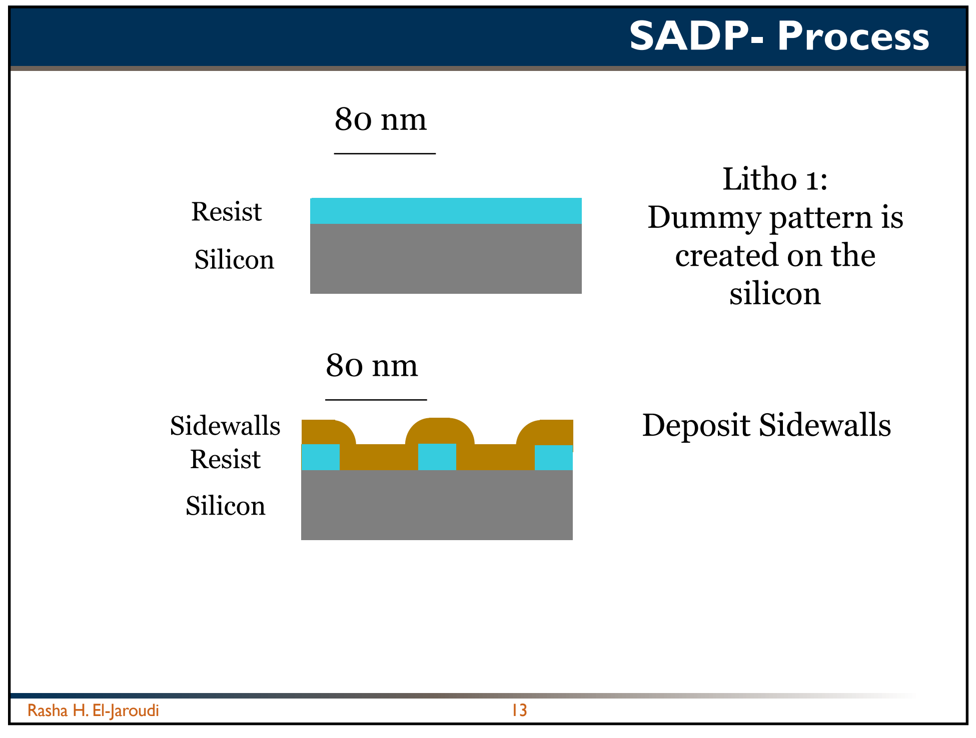
LELE- Challenges Cont.

- Mask Overlap
  - Ideally would need no overlap
  - Need to compensate for trench pull back
- Mask Overlay Issues
  - Misalignment can severely affect the device's reliability

Ideal Overlay

5-7 nm Overlay Error

1. V. Wiaux et al. Proc. of SPIE Vol. 6924, 692409, (2008)
2. Yan Borodovsky, Intel, 2012 International Workshop on EUV Lithography.


SADP- Process
80 nm
Resist
Silicon
Litho 1:
Dummy pattern is created on the silicon
80 nm
Sidewalls
Resist
Silicon
Deposit Sidewalls
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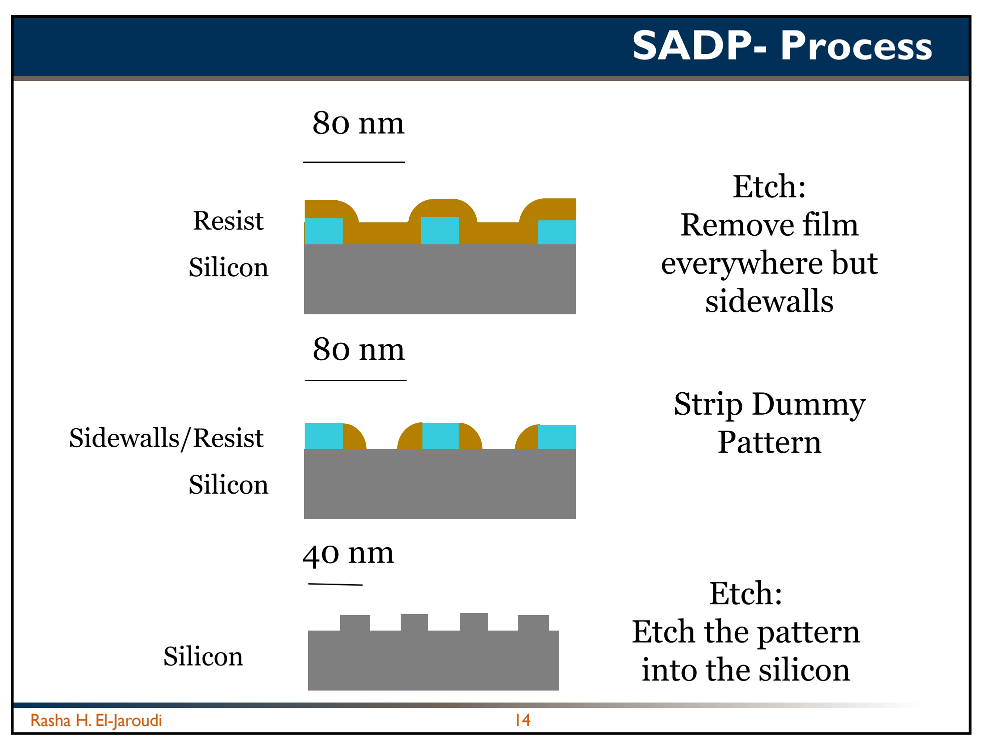
SADP- Process
80 nm
Resist
Silicon
Etch:
Remove film everywhere but sidewalls
80 nm
Sidewalls/Resist
Silicon
Strip Dummy Pattern
40 nm
Silicon
Etch:
Etch the pattern into the silicon
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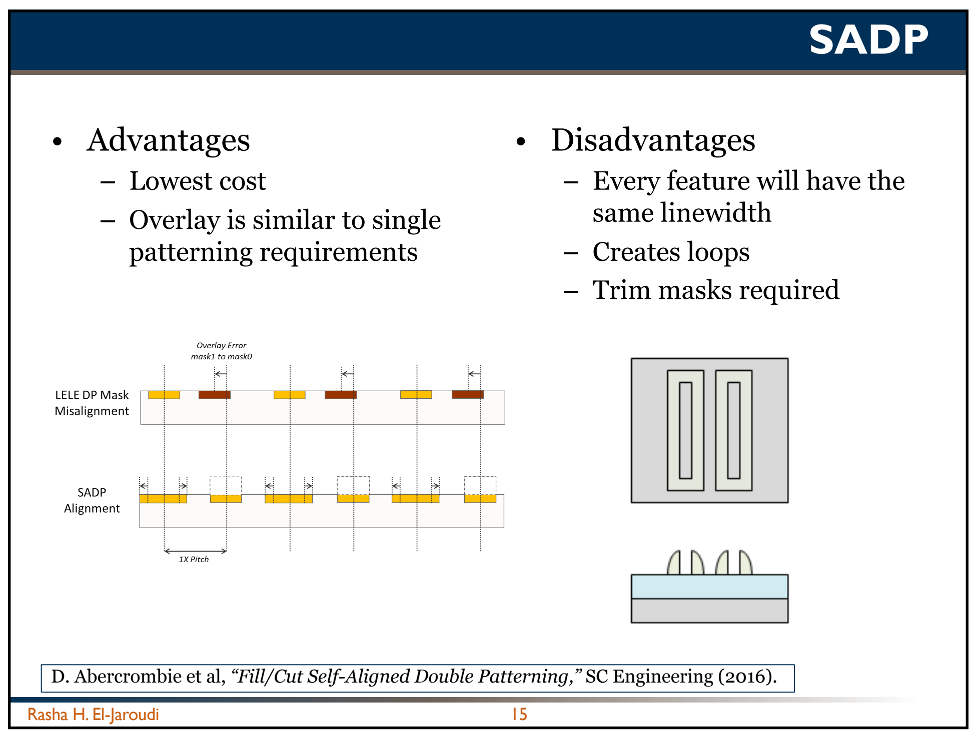
SADP
Advantages
Lowest cost
Overlay is similar to single patterning requirements
Disadvantages
Every feature will have the same linewidth
Creates loops
Trim masks required
Overlay Error mask1 to mask0
LELE DP Mask Misalignment
SADP Alignment
1X Pitch
D. Abercrombie et al, "Fill/Cut Self-Aligned Double Patterning," SC Engineering (2016).
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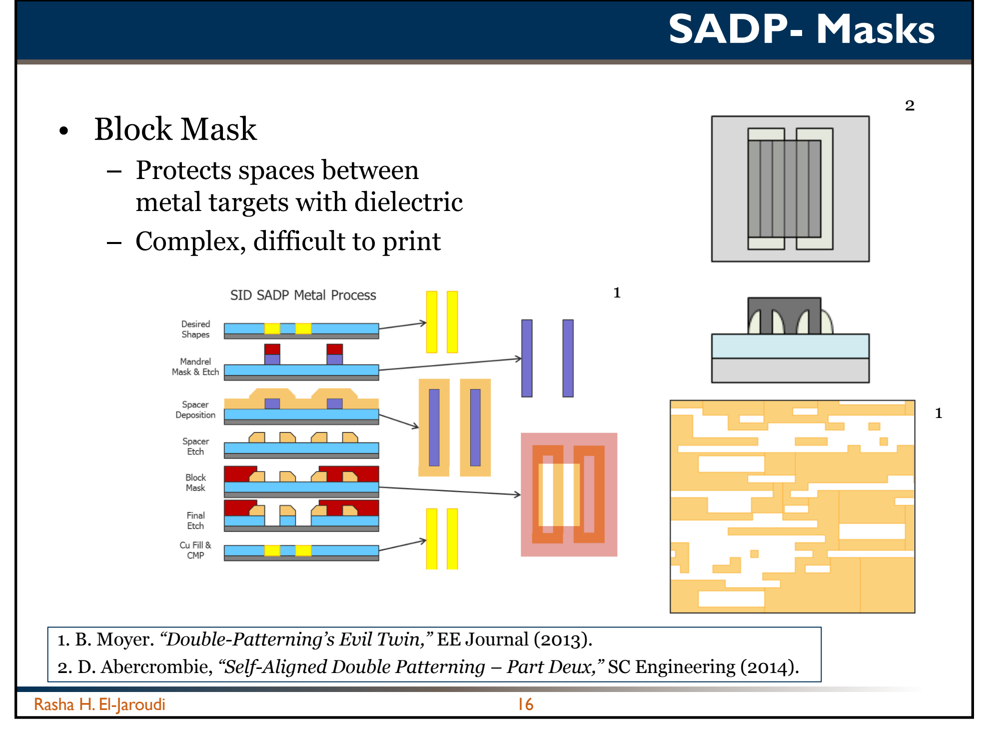
SADP- Masks
Block Mask
Protects spaces between metal targets with dielectric
Complex, difficult to print
SID SADP Metal Process
Desired Shapes
Mandrel Mask & Etch
Spacer Deposition
Spacer Etch
Block Mask
Final Etch
Cu Fill & CMP
1
2
1
1. B. Moyer. "Double-Patterning's Evil Twin," EE Journal (2013).
2. D. Abercrombie, "Self-Aligned Double Patterning – Part Deux," SC Engineering (2014).
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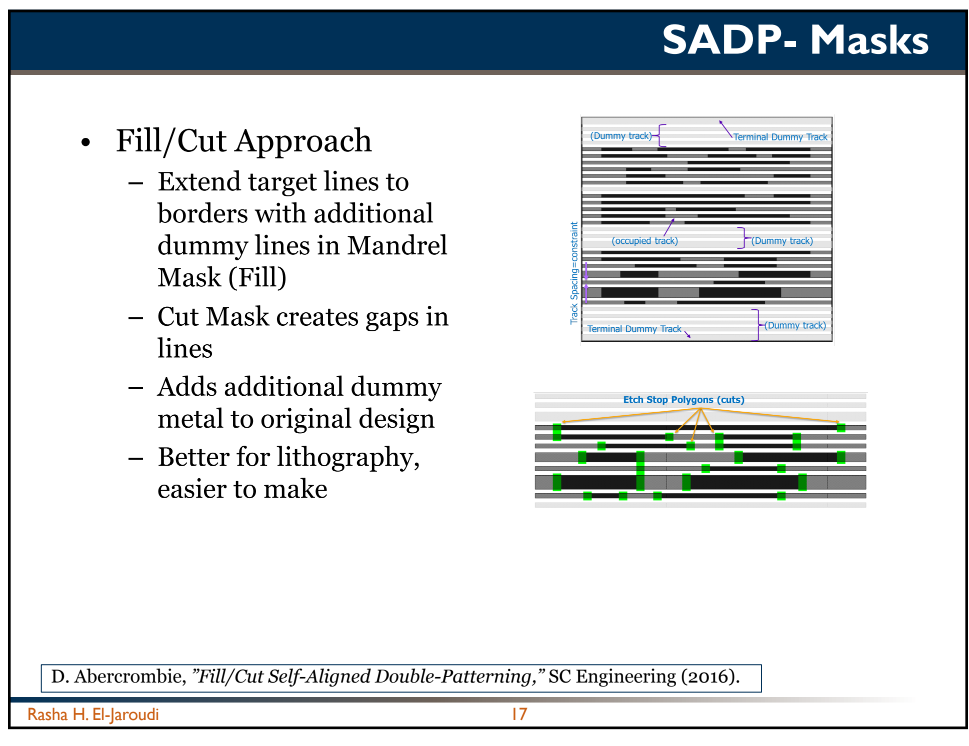
SADP- Masks
• Fill/Cut Approach
– Extend target lines to borders with additional dummy lines in Mandrel Mask (Fill)
– Cut Mask creates gaps in lines
– Adds additional dummy metal to original design
– Better for lithography, easier to make
(Dummy track)
Terminal Dummy Track
(occupied track)
(Dummy track)
Track Spacing=constraint
Terminal Dummy Track
(Dummy track)
Etch Stop Polygons (cuts)
D. Abercrombie, "Fill/Cut Self-Aligned Double-Patterning," SC Engineering (2016).
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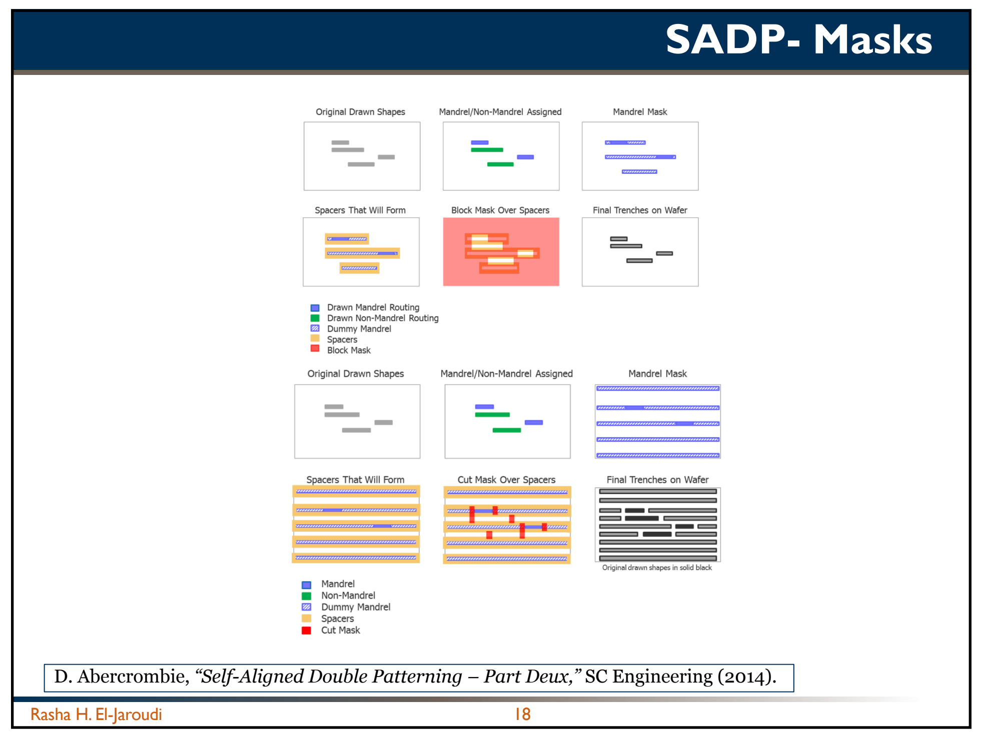
SADP- Masks
Original Drawn Shapes
Mandrel/Non-Mandrel Assigned
Mandrel Mask
Spacers That Will Form
Block Mask Over Spacers
Final Trenches on Wafer
Drawn Mandrel Routing
Drawn Non-Mandrel Routing
Dummy Mandrel
Spacers
Block Mask
Original Drawn Shapes
Mandrel/Non-Mandrel Assigned
Mandrel Mask
Spacers That Will Form
Cut Mask Over Spacers
Final Trenches on Wafer
Original drawn shapes in solid black
Mandrel
Non-Mandrel
Dummy Mandrel
Spacers
Cut Mask
D. Abercrombie, "Self-Aligned Double Patterning – Part Deux," SC Engineering (2014).
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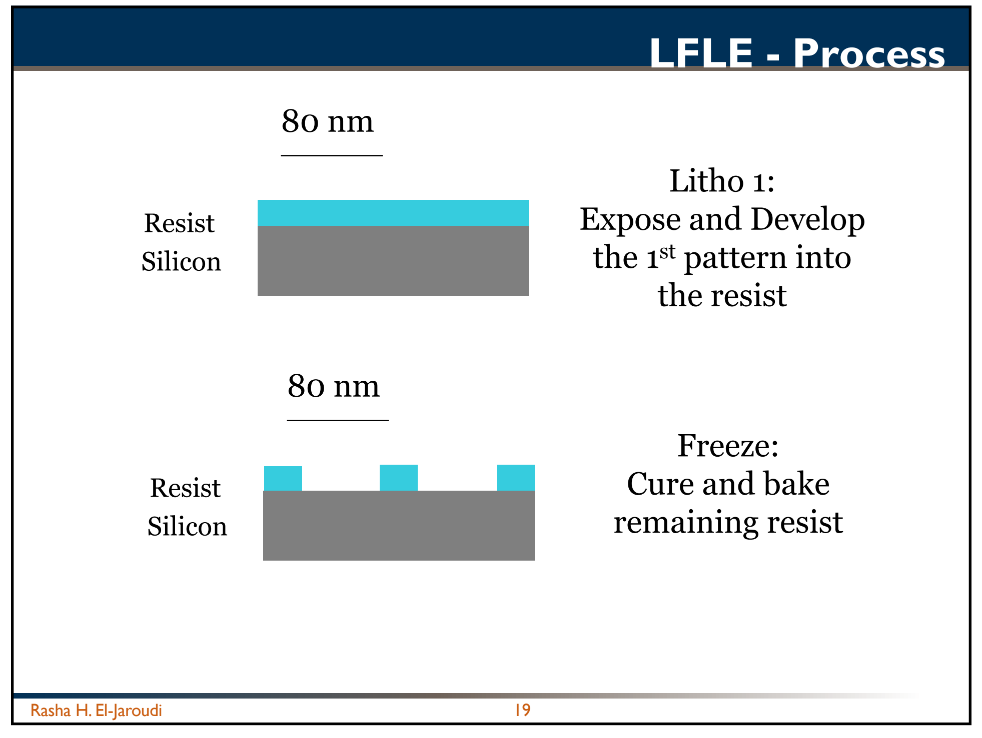
LFLE - Process
80 nm
Resist
Silicon
Litho 1:
Expose and Develop the 1st pattern into the resist
80 nm
Resist
Silicon
Freeze:
Cure and bake remaining resist
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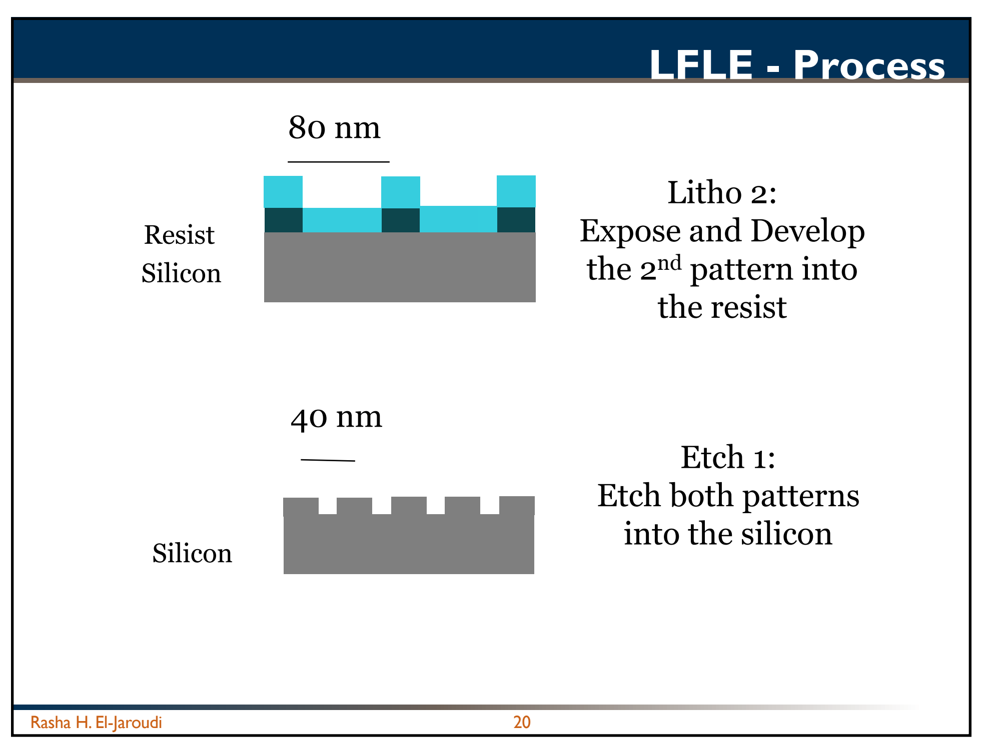
LFLE - Process
80 nm
Resist
Silicon
Litho 2:
Expose and Develop the 2nd pattern into the resist
40 nm
Silicon
Etch 1:
Etch both patterns into the silicon
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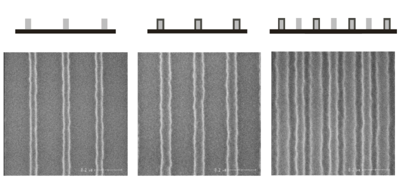
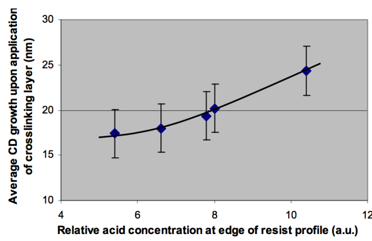
LFLE

- Advantages
  - Reduces number of steps
  - Increases throughput
  - All steps can be carried out in the same system
- Challenges
  - Existence of freezing material
  - Same overlay issues as LELE

LFLE- Protective Coating

- Cover first pattern with protective material, acid in protective coating diffuses into resist and crosslinks features
- Causes CD growth of 15-25 nm
  - Reduces double patterning pitch reduction
  - 1st and 2nd lines will be different sizes
- Difficult to fix using OPC
  - CD growth dependent on exposure energy in addition to pitch and mask CD





A. Vanleehove et al. Proc. of SPIE Vol. 6520 65202F-1

LFLE- UV Curing

- 193nm
  - Increasing dose, suppresses swelling but increases resist flow
- 172nm
  - Suppresses swelling without causing reflow
  - Need to cure and bake to prevent 1st resist distortion during 2nd resist process
- Causes CD shifts, line-end shortages, and corner feature deformation

Increasing cure dose, 170 °C cure bake.

193 nm Flood

172 nm Flood

N. Bekiaris et al. Proc. of SPIE Vol. 6923 692321-4

Double Patterning Summary

- Litho-Etch-Litho-Etch
  - First double patterning technique
  - Successfully reduces k_1 below previous limit
  - Doubles the processing steps, so doubles the cost and reduces throughput
  - Requires a hard mask
  - Suffers from mask overlay issues

LITHO-ETCH-LITHO-ETCH (LELE)

1 Litho 1. The first pattern [yellow] is exposed onto a hard mask.

2 Etch 1. The first pattern is etched into the hard mask [brown].

3 Litho 2. A second pattern [yellow] is exposed onto silicon [blue], doubling pattern density.

4 Etch 2. The final, double-density pattern is engraved into the silicon.

5 Wash. The remaining mask is washed away.

C. Mack, *"Seeing Double,"* IEEE Spectrum (2008).

Double Patterning Summary Cont.

- Self-Aligned Double Patterning
  - Developed in response to LELE's mask overlay issues
  - Single lithography step
  - Need to use an additional block or cut mask to remove unwanted material
  - Complicated to design masks for SADP
  - Process intensive

SIDEWALL SPACER

1 **Litho + Etch 1 (dummy patterns).** A dummy pattern [yellow] is created on silicon [blue].

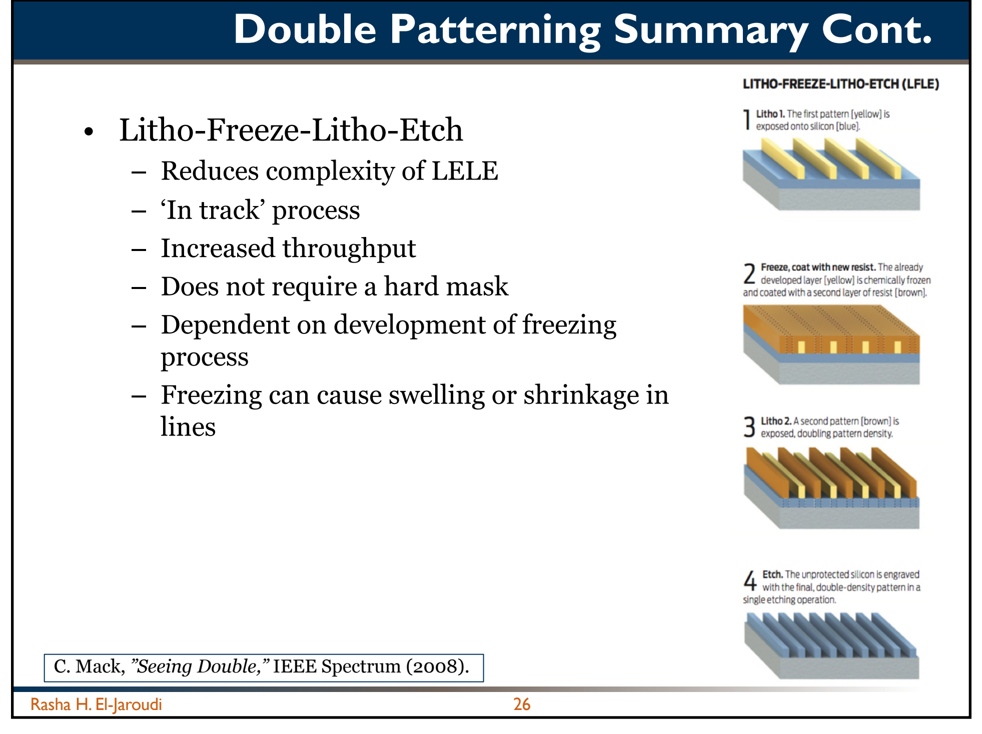
2 **Grow sidewalls.** A film [brown] is grown around the dummy lines.

3 **Etchback.** All of the film is removed except the sidewalls.

4 **Strip dummy pattern.** The dummy pattern [yellow] is removed, leaving the sidewalls.

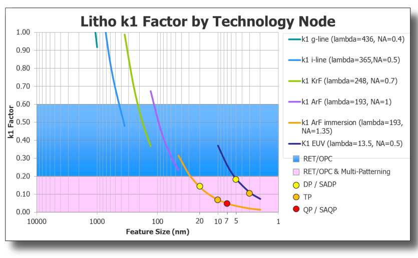
5 **Etch 2.** The remaining double-density sidewa pattern is etched into the silicon [blue].

C. Mack, *"Seeing Double,"* IEEE Spectrum (2008).



Double Patterning Summary Cont.

- No perfect technique
- Splitting and designing double exposure masks is non trivial
- Not all images can be successfully split for double exposure
- No single exposure option, yet



D. Abercrombie, *"Will EUV Kill Multi-Patterning,"* SC Engineering (2017).

Outline

- Motivation
- Techniques
- **Future of Double Patterning**

What about EUV Lithography?

- EUV wavelength is 13.5nm
- In 2014, ASML said EUV is coming between 2019-2024
  - 3nm nodes
  - 200 W/hr
- 7nm nodes
  - 34 Lithography steps with multi-patterning
  - 9 Lithography steps with EUV
- EUV may not be ready until 5nm nodes
  - Requires multi-patterning with EUV

M. Van den Brink, AMSL Small Talk 2014.

Comparing Costs

Patterning Technique	Normalized Wafer Cost
193i SE	1
193i SADP	2
193i LELE (DP)	2.5
193i SAQP	3
193i LELELE (TP)	3.5
EUV SE	4
EUV SADP	6

A. Raley et al., Proc. SPIE 9782, 97820F (2016).