Employing Step and Flash Imprint Lithography for Gate Level Patterning of a MOSFET Device

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ABSTRACT

Step and Flash Imprint Lithography (SFIL) is an alternative lithography technique that enables patterning of sub-100 nm features at a cost that has the potential to be substantially lower than either conventional projection lithography or proposed next generation lithography techniques. SFIL is a molding process that transfers the topography of a rigid transparent template using a low-viscosity, UV-curable organosilicon solution at room temperature and with minimal applied pressure.[1] Employing SFIL technology we have successfully patterned areas of high and low density, semi-dense and isolated lines down to 20 nm,[2] and demonstrated the capability of layer-to-layer alignment.[3] We have also confirmed the use of SFIL to produce functional optical devices including a micropolarizer array consisting of orthogonal 100 nm titanium lines and spaces fabricated using a metal lift-off process.[4] This paper presents a demonstration of the SFIL technique for the patterning of the gate level in a functional MOSFET device.

Keywords: Step and Flash Imprint Lithography, Alignment, Planarization, Etching, MOSFET

1. INTRODUCTION

Step and Flash Imprint Lithography (SFIL) is a low-cost, high throughput approach to fabricating features in the sub-100 nm regime. SFIL differs from conventional lithography techniques in that it does not use projection optics or complex lenses, thereby significantly reducing the capital cost of the equipment. The process operates at room temperature and makes use of chemical and low pressure mechanical processes to transfer patterns. Many nano-imprint lithography processes have emerged over the last few years, all of which use the topography defined on a template to create a pattern on a substrate.[5-9] SFIL differs from these other techniques in that it uses a low viscosity, photocurable liquid and a transparent template eliminating the need for high temperatures and pressures. This alleviates concerns with overlay alignment accuracy and the effects of the thermal cycle times on the imprint process.

The SFIL process is illustrated in Figure 1. A silicon substrate is first spin-coated with an organic transfer layer. Then a small amount of low viscosity, photopolymerizable, organosilicon solution (etch barrier) is dispensed onto the wafer in the area to be imprinted. The etch barrier formulation used in these experiments consisted of 15%(w/w) ethylene glycol diacrylate (Aldrich), 44% (3-acryloxypropyl)tris(trimethylsiloxy)silane (SIA0210.0, Gelest), 37% t-butyl acrylate (Lancaster), and 4% 2-hydrozy-2-methyl-1-phenyl-propan-1-one (Darocur 1173, Ciba). A template bearing 1X patterned relief structures, written by electron beam lithography[2] and surface-treated[10] with a fluorocarbon film, is aligned over the dispensed solution and lowered to make contact to the substrate. This displaces the etch barrier and fills the patterned relief structures on the template. Once filling has occurred, the area is irradiated with broadband ultraviolet light through the back side of the template and cross-linking of the polymer occurs. The template is then separated from the substrate, leaving an organosilicon relief pattern identical to the template relief pattern. The etching is performed in a two-step process. The first is a halogen etch that is referred to as the "breakthrough etch" because it is used to break through the undisplaced etch barrier and expose the underlying organic transfer layer. Finally, an anisotropic oxygen reactive ion etch is then used to transfer the imprinted features to the underlying substrate.

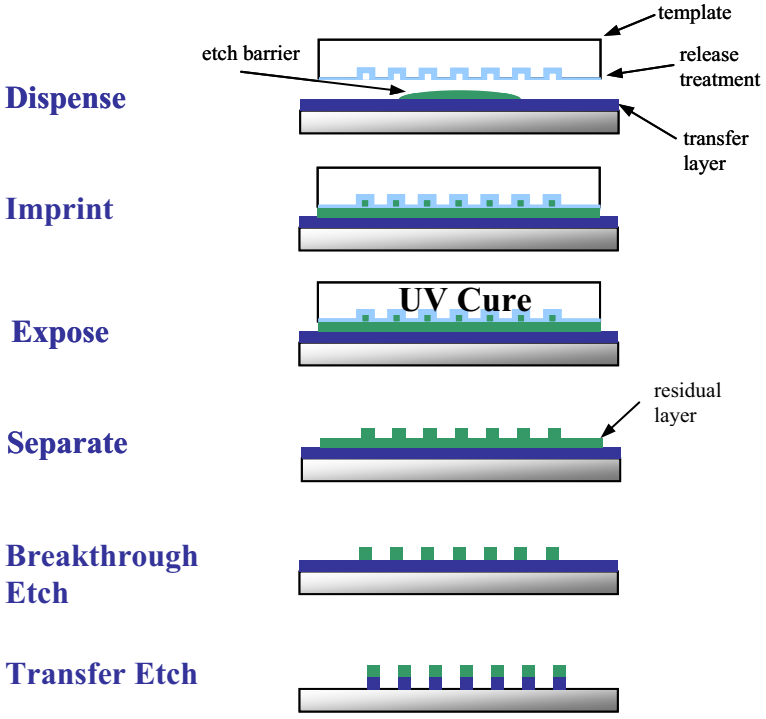

Figure 1. The Step and Flash Imprint Lithography process

The incorporation of the SFIL process in the fabrication of a metal oxide semiconductor field effect transistor (MOSFET), presented many challenges. A planarization process and the ability to perform layer-to-layer alignment through the template have been demonstrated. This paper describes these challenges and the steps taken to fabricate the first working electrical device using SFIL technology. For proof of concept purposes SFIL was used only for the most critical dimension in the MOSFET process flow; the fabrication of the gate level.

2. SFIL GATE FABRICATION PROCESS FLOW

Figure 2(a) shows a simplified MOSFET process flow for the fabrication of the transistor gate. In this process, the starting substrate is a wafer on which the field oxide and the gate oxide have been grown, the poly-Si deposited, and the oxide hard mask is in place. This would be spin-coated with resist, exposed, and developed leaving the patterned resist features. These resist features then serve as an etch mask used to pattern the hard mask that is ultimately the pattern that defines the underlying poly-Si for the transistor gate. The SFIL technique replaces the spin-coating and exposing steps used in conventional lithography with the process flow seen in Figure 2(b) and described below.

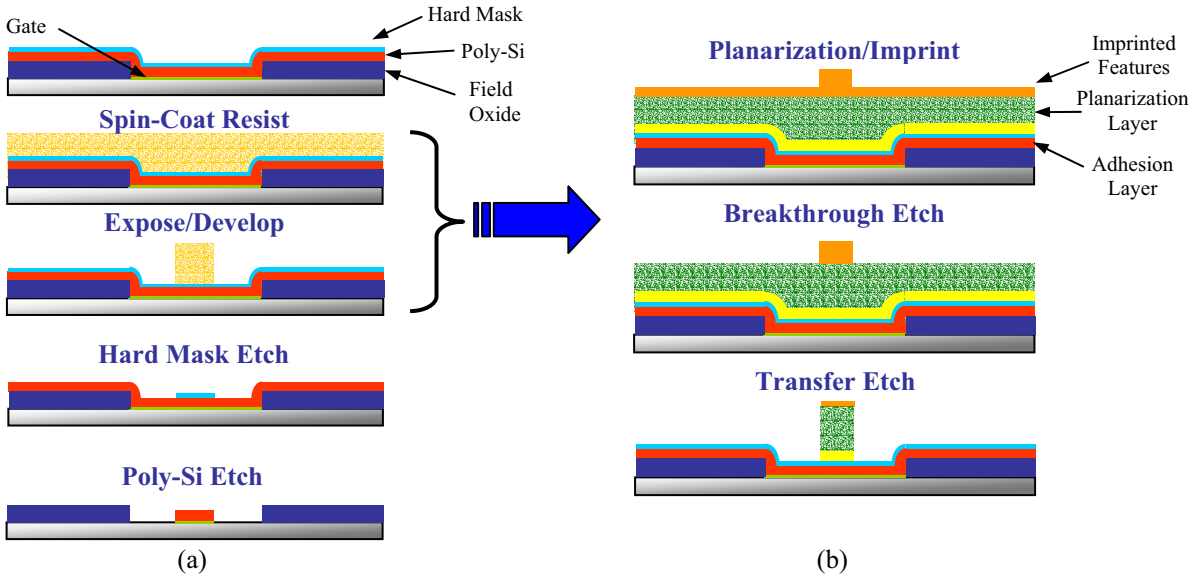

Figure 2. (a) Simplified industry MOSFET process flow for gate fabrication.
(b) Additional steps employed by SFIL.

2.1. Planarization

The incorporation of an organic planarization layer (transfer layer) that is imprinted with a featureless template to normalize the effects of the underlying topography on the imprint surface has been detailed previously.[4] For this application, the 250 nm step generated during the growth of the field oxide needed to be planarized in order to allow gate pattern imprinting. This was achieved by first spin-coating the substrate with poly(hydroxystyrene) (PHS). To provide a conformal coating across the wafer that averaged 200 nm in thickness. PHS also provided an adhesion medium for the planarization layer that was found to have poor adhesion to the oxide surface.

Following the conformal coating of the PHS adhesion layer, an imprint was performed to planarize the surface. This was done by first manually dispensing a small amount of ethylene glycol diacrylate (Aldrich) containing a photoinitiator and imprinting with a blank, featureless, optically flat template. The imprint was performed using the automated SFIL Multi-Imprint Machine at the University of Texas, which has been described previously.[11] Planarization of the underlying topography was confirmed using a KLA-Tencor Alphastep 200 profilometer. This planarization layer also served as the transfer layer described earlier in the SFIL process. The film had an average thickness of 700 nm. A scanning electron microscopy image (SEM) of the planarization layer is shown in Figure 3.

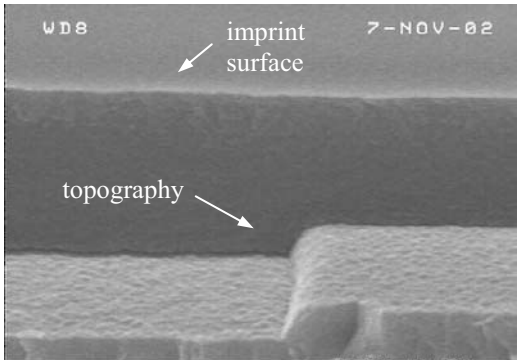

Figure 3. Planarization layer over underlying 250nm topography.

2.2. Alignment and Imprinting

The ability to perform alignment in SFIL has been described in detail previously.[3] This work was performed on a Canon 501 mask aligner at that has been modified for the SFIL process. This tool employs optical microscopy to detecting alignment error, making the corresponding corrections in X, Y, and theta, and performing the UV exposure to complete the imprint. The process was performed by dispensing a small amount of etch barrier on the wafer in the area to be imprinted. The wafer was then raised on a hydraulic piston into close proximity of the template. As the etch barrier filled the template relief patterns, a thin layer of fluid prevents the wafer from actually making contact with template. This thin fluid film, referred to as the residual layer, acts as both a lubricant and a damping agent allowing adjustment in the alignment to be made. The alignment marks on the wafer surface and the template can be viewed through the backside of the template and fine alignment was performed with minimal optical errors.

Alignment between the underlying poly-Si and the SFIL patterned template was required to define the gate structures over the active areas of the wafer. Rough alignment in the theta direction was performed using a simple cross-in-box pattern. The cross feature was previously defined on the wafer surface and the box pattern was present in the relief image on the template. Fine alignment was performed using Vernier marks in the X and Y directions. With the center marks on the vernier aligned, the resulting overlay error was found to be less than 0.25μm. Following alignment, the imprint area was irradiated with UV light, polymerizing the etch barrier and leaving an organosilicon relief image that is a replica of the template pattern.

2.3. Etching

Transferring the imprinted pattern to the underlying substrate required a two step etch process. Both processes are derivatives of commonly used etch processes and do not require the addition of any exotic etch gases. The final etch profiles are high-aspect ratio, organic features analogous to patterned resist features in conventional lithography. The etching done in this research was performed on a PlasmaTherm 790 Series reactive ion etcher (RIE).

An anisotropic halogen RIE rich in fluorine was used to break-through the residual layer exposing the underlying transfer layer. This etch was performed with a combination of 30 standard cubic centimeters per minute (sccm) CHF_3 and 5 sccm O_2 at a pressure of 17 mTorr and RF power of 450W. The use of a halogen gas, CHF_3 in this case, is

required by the organosilicon nature of the etch barrier. This etch is similar to a standard SiO_2 etch that would be performed in modern integrated circuit (IC) processing. Following the break-through etch, the remaining silicon-containing features serve as an etch mask to transfer the pattern to the underlying substrate. This "transfer etch" was achieved with a standard, anisotropic, oxygen RIE using 8 sccm O_2 at 5 mTorr and RF power of 400W. An SEM image of a polymer gate structure after both the breakthrough and transfer etch is shown in Figure 4.

The etcher used in these experiments was not equipped with an end-point detection system. Therefore, each etch had to be performed for a set period of time based on the measured etch rates and estimated residual layer thickness. The etch rates were determined experimentally by masking off a portion of the imprinted area with a piece of another wafer and etching for varying lengths of time. Each sample was examined with a profilometer and confirmed via cross-sectional images on a SEM. The etch rate of the etch barrier was found to be approximately 90 nm/min while the EGDA and the PHS etched at rates of 80 nm/min and 45 nm/min, respectively.

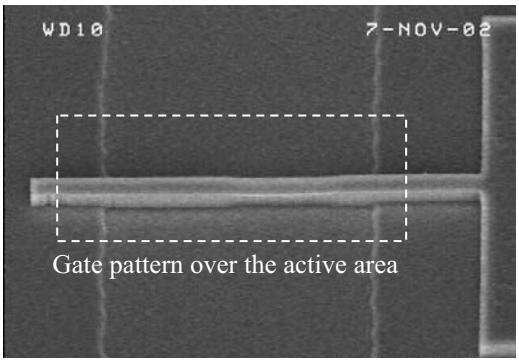

Figure 4. Gate pattern following the breakthrough etch and transfer etch.

Following the transfer of the feature to the underlying substrate, standard etch processes were used to pattern the hard mask and the poly-Si. The hard mask etch uses halogen etch chemistry and the standard poly-Si etch incorporated a combination of bromine and chlorine.

3. RESULTS

3.1. Completed MOSFET Device

The remaining steps in the fabrication of this MOSFET device were completed using conventional processing techniques. Following gate patterning, each wafer underwent implantation, isolation oxide growth, contact patterning, and aluminum deposition. An example of one of the completed devices used in these experiments is shown in Figure 5. These devices were made with a process that did not incorporate an anti-punch-through implant, source/drain extensions, or silicide gate cap, features that are required to get good performance from short gate lengths. These steps are within our processing capability and will be included in future device fabrication processes.

3.2. Electrical Data

Following processing, the completed devices were electrically tested. Both drain current vs. drain voltage (I_d vs. V_d) and drain current vs. gate voltage (I_d vs. V_g) curves were obtained and can be seen in figures 6 and 7, respectively. These I-V curves confirm the functionality of the fabricated MOSFET devices and the successful incorporation of SFIL in creating a working electrical device. The electrical data are also consistent with other electrical devices fabricated with conventional lithographic techniques using similar processing equipment.

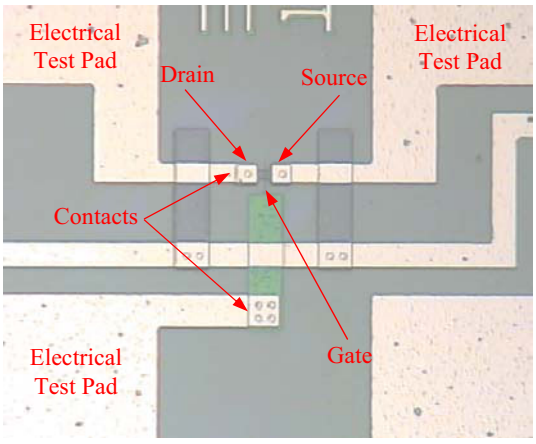

Figure 5. Completed MOSFET device.

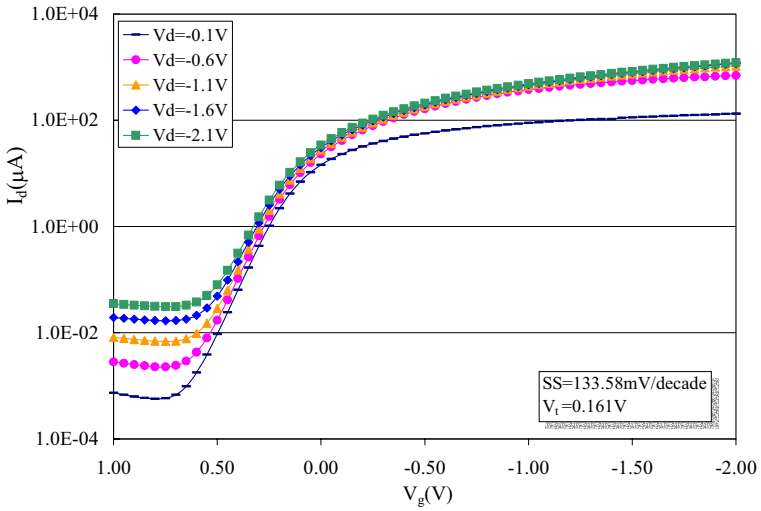

Figure 6. I_d vs V_g curves of SFIL PMOSFET, L=2μm, W=23μm

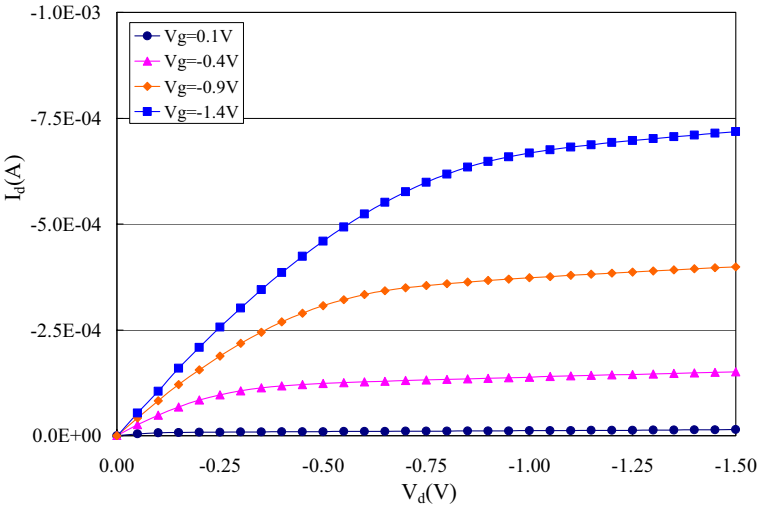

Figure 7. I_d vs V_d curves of SFIL PMOSFET, L=2μm, W=23μm

4. CONCLUSIONS

Step and Flash Imprint Lithography is capable of producing an electrical device. This implies that none of the SFIL processing steps impair its ability to fabricate a working MOSFET transistor. The low pressure, room temperature nature of the SFIL process and the use of transparent imprint templates that enables layer-to-layer alignment makes SFIL particularly well suited for patterning critical features. In this paper, we have confirmed the use of a planarization layer to normalize local topography, demonstrated layer-to-layer alignment of critical features, and developed the etch processes to transfer high-aspect ratio features. Planarization was achieved by imprinting an organic photocurable solution with a featureless template. Overlay alignment was performed through the template by superimposing the alignment marks on the template with the marks on the wafers. Etching was completed with a two step etch process that involved a halogen break-through etch followed by an oxygen RIE transfer etch. The completed MOSFET devices were electrically tested and the corresponding I-V curves confirm the functionality of these devices.

The objective of this research was to demonstrate the use of SFIL in the fabrication of a working electrical device. Another template is being generated that will include 30 nm transistor gates patterns. The acquisition of this template and access to an etcher with a higher degree of anisotropy and an end-point detection system will enable us to use SFIL to produce functional MOSFET devices with gate lengths in deep sub-100 nm regime.

5. ACKNOWLEDGMENTS

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