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**Development of a Baseline Process for the Integration of Step and
Flash Imprint Lithography into a MOSFET Fabrication Process**

by

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Thesis

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**Development of a Baseline Process for the Integration of Step and
Flash Imprint Lithography into a MOSFET Fabrication Process**

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Abstract

Development of a Baseline Process for Integrating Step and Flash Imprint Lithography into a MOSFET Fabrication Process

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This thesis presents the results of process development for using Step and Flash* Imprint Lithography (S-FIL*) to pattern the gate structures of MOSFETs. S-FIL is a replication technique with sub-50nm resolution capability that has the potential to provide a low cost, high throughput pattern replication process. Imprint lithography techniques are essentially micro-molding processes in which the topography of a template defines the patterns created on a substrate. S-FIL is an imprint lithography technique that operates at room temperature and low pressures and is based on a low-viscosity, UV-curable liquid approach. This approach is particularly suited for high-resolution layer-to-layer alignment.

The general processes used to incorporate the S-FIL into the MOSFET process flow were planarization, alignment and imprint, and reactive ion etching (RIE). The S-FIL processing was used in the MOSFET process flow after the

* “Step and Flash” and “S-FIL” are trademarks of The University of Texas System.

gate oxide, Poly-Si, and oxide hard mask layers were deposited on top of a low-resolution active-patterned isolation oxide. The topography was planarized using a combination of spin-coating and the S-FIL planarization process with a featureless template. Imprinting was done with sub-micron alignment using through-the-template optical feedback. Anisotropic reactive ion etching was used to transfer the pattern; first a halogen de-scum etch, followed by an oxygen etch of the organic planarization layers. The organic planarization layers were designed to mask the oxide hard mask.

Table of Contents

List of Tables	x
List of Figures.....	xi
List of Figures.....	xi
Chapter 1: Background	1
1.1 Introduction	1
1.2 Step and Flash Imprint Lithography (S-FIL).....	4
1.3 Si-Ge-C MOSFET Process Development Project	6
1.3.1 Motivation for Si-Ge-C and S-FIL (This section is adapted from Onsongo, 2001).....	7
1.3.2 Si-Ge-C MOSFET Fabrication Process.....	10
1.3.3 ACTIVE Patterned Topography.....	12
1.3.4 ACTIVE and POLY Patterns	13
1.4 Thesis Overview.....	18
Chapter 2: Planarization.....	21
2.1 Introduction	21
2.2 Need for Planarization for S-FIL integration into MOSFET fabrication process	21
2.2.1 Minimize the Break-through Etch.....	22
2.2.2 Feature Preservation Over Topography.....	24
2.3 Requirements for Planarization.....	26
2.3.1 Planarize the Area of One MOSFET	27
2.3.2 Planarize the Largest Active Area	28
2.3.3. Maximum and Minimum Thickness	28
2.3.4 Contamination Issues.....	29
2.3.5 Thickness Can Be Measured Accurately.....	29
2.3.6 Be Readily Etched in O ₂ Plasma	30

2.3.7 Good Adhesion.....	31
2.3.8 Not Mix with the Etch Barrier	31
2.3.9 Four-Inch Wafers.....	32
2.3.10 Flatness Variation.....	32
2.4 Planarization Background and Alternatives	37
2.4.1 Spin-Coating.....	39
2.4.2 Spin-Coating with Reflow.....	42
2.4.3 Spin-Coating with Etch-back	43
2.4.4 Chemical-Mechanical Polishing.....	43
2.4.5 Contact Planarization.....	44
2.5 Planarization Experiments	47
2.5.1 Spin-Coating Experiments.....	47
2.5.2 Spin-Coating and Reflow.....	52
2.5.3 Spin-Coating and Imprinting.....	55
Chapter 3: Imprinting and Alignment	68
3.1 Introduction	68
3.2 Goals of imprinting and alignment	68
3.3 S-FIL Overlay Alignment Machine (OAM).....	70
3.4 Imprinting and Alignment Process	73
3.5 Results	75
3.5.1 Uniformity of imprints	75
3.5.2 Alignment results.....	79
Chapter 4: Etching.....	81
4.1 Introduction	81
4.2 Reactive-Ion Etching	81
4.3 Background on the etching needed for S-FIL	84
4.4 Grass Problem	90
4.5 CD loss measurement.....	96

4.6 Predicted Etch Transfer	101
Chapter 5: Conclusions and Future Work	104
5.1 Conclusions	104
5.1.1 Overview	104
5.1.2 Planarization.....	104
5.1.3 Imprinting and Alignment	105
5.1.4 Etching.....	106
5.2 Future Work.....	107
5.2.1 Improve the Alignment Scheme	107
5.2.2 Decrease Barli Layer Thicknesses.....	107
5.2.3 Exclude Spin-coating.....	108
5.2.4 Decrease Planarizing Imprint Shrinkage	109
5.2.5 Materials Development	109
5.2.6 Etching Anisotropy.....	109
5.2.7 Improve Imprint Thickness and Uniformity.....	110
5.2.8 Complete the Process	110
References	111
Vita	114

List of Tables

Table 2.1. Planarization results from spin-coating HR100 and Barli.....	52
Table 2.2. Planarization results from spin-coating novolak and positive photoresist and allowing to reflow.	55
Table 4.1. Parameters used to calculate the range of thickness of residual layer that will transfer imprinted patterns.	102

List of Figures

Figure 1.1. Historical data for the number of transistors per chip and minimum feature size for lithography, logic density, and memory density.....	3
Figure 1.2. The Step and Flash Imprint Lithography process.	6
Figure 1.3. Si-Ge-C MOSFET Design.	9
Figure 1.4. Si-Ge-C MOSFET Fabrication Process Flow.	11
Figure 1.5. SEM image of cross-section wall slope to ACTIVE pattern area.....	13
Figure 1.6. Schematic of a 4” wafer showing the placement of dies of the lithography patterns, the orientation of the dies, and the position of the rows of MOSFETS.....	14
Figure 1.7. Schematic showing the arrangement of the rows of MOSFET on a die, with their respective gate lengths.....	16
Figure 1.8. Optical Images showing a row of the ACTIVE pattern (upper) and a row of the POLY pattern (lower).....	17
Figure 1.9. Top-down SEM images showing the range of sizes of areas to be planarized on the ACTIVE pattern. The left and right images are for MOSFET with 23 and 3 micron gates widths, respectively.	17
Figure 1.11. S-FIL Processes for Integration into Si-Ge-C MOSFET Fabrication Process.....	19
Figure 2.1. Planarization is desired for minimizing the break-through etch.	24
Figure 2.2. Planarization is needed for feature preservation over topography.	26

Figure 2.3. Schematic showing imprint on planarization layer, used to determine variation in flatness requirement and define terms.....	33
Figure 2.4. Surface after break-through etch shown to document surface roughness.....	35
Figure 2.5. Definition of percent planarization.	38
Figure 2.6. A single die showing where the thickness and planarization measurements were taken.	59
Figure 2.7. Profilometer scans showing the progression of planarization with Barli, CHA Imprint, and then Barli.	60
Figure 2.8. Profilometer scans showing the progression of planarization with Barli, XCHA Imprint, and then Barli.	62
Figure 2.9. Image of a photograph showing a planarizing imprint on the ACTIVE pattern, also designating the numbering of dies 1-3.	63
Figure 2.10. Thickness variation of planarized layers across the measured side of dies 1-3.	64
Figure 2.11. Planarization variation with Barli, XCHA Imprint, and Barli across the measured side of dies 1-3.	65
Figure 2.12. Cross-sectional view showing the thickness of the planarization layers.....	66
Figure 2.13. Transfer of a dot structure through the planarization layers.	67
Figure 3.1. Definitions of directions of coordinates used in this chapter.	69

Figure 3.2. Two views of the S-FIL OAM – with the microscope and exposure assembly pivoted to the side (left) and directly over the wafer (right).	71
Figure 3.3. The S-FIL tip/tilt flexure assembly (left) and template holder (right).	71
Figure 3.4. Microscope image of an aligned imprint above the active pattern, showing the alignment marks.	75
Figure 3.5. Images of a wafer shown for thickness uniformity approximation with planarization imprint (left) and subsequent POLY patterned imprint.	76
Figure 3.6. Cross-section SEM of an imprints in two locations 0.25 mm apart, showing little difference in etch barrier residual layer and planarization layer thickness.	78
Figure 3.7. Microscope images showing the alignment marks from imprint shown in Figure 3.5.	79
Figure 3.8. Microscope images showing imprinted gates structures aligned over active areas from imprint shown in Figure 3.5.	80
Figure 4.1. Schematic of the reactive-ion etching system used.	84
Figure 4.2. Etch processes needed for S-FIL integration into the MOSFET fabrication process.	86
Figure 4.3. SEM image of an imprinted dot-tower (unetched).	88
Figure 4.4. SEM image of an imprinted dot-tower after a break-through etch.	89
Figure 4.5. SEM image of a Barli film (unetched).	89

Figure 4.6. SEM image of an imprinted dot-towers after the break-through etch and the oxygen etch.	90
Figure 4.7. SEM images of imprinted dot patterns after the halogen etch (July17 images 1 and 2).....	91
Figure 4.8. SEM images of imprinted dot patterns after the halogen etch and oxygen etch.	92
Figure 4.9. SEM image of a wafer with Barli that was oxygen etched, showing grass.	95
Figure 4.10. XPS data showing 6% atomic concentration of aluminum on the etched Barli sample.	95
Figure 4.11. SEM image of the dot-tower pattern with lines showing how a wafer could be diced for CD loss measurement.	97
Figure 4.12. CD loss/Thickness of Material Etched for the halogen and oxygen etch processes used.	99

Chapter 1: Background

The resolution capability of photolithography is steadily increasing, but the cost of photolithography tools is exponentially increasing also. Step and Flash Imprint Lithography (S-FIL) is potentially a low-cost, ultra high-resolution semiconductor fabrication technology, a nano-patterning technique that uses a low-viscosity liquid at low pressures and room temperature that cures when exposed to UV light. This research addresses the development of a basic approach to integrating S-FIL into a metal-oxide-semiconductor field-effect transistor (MOSFET) fabrication process.

1.1 INTRODUCTION

The microelectronic industry standard for pattern generation is photolithography (or optical lithography). In order to satisfy the need for faster and cheaper chips, optical lithography must be able to produce smaller devices by using tools capable of generating patterns with higher resolution. Optical lithography uses projection optics to transfer a pattern that is on a lithography mask onto wafers. This information transfer is done in parallel, and is a high-throughput process. The masks are patterned by direct-write laser tools or electron beam (EBEAM) lithography tools, where the information is transferred into the mask in series, and is a much slower process. EBEAM lithography can transfer patterns with features smaller than 50 nm [Resnick et al. 2002], but is generally not used to pattern wafers because of its unacceptably low-throughput.

Although EBEAM lithography can make masks with 50 nm features, the projection optics of photolithography cannot transfer features smaller than the resolution limit of optical projection systems to wafers. The resolution limit of projection optical systems is characterized by the Rayleigh formula [Thompson, Bowden, and Willson 1994],

$$D \approx k \frac{\lambda}{NA}$$

where D is the minimum dimension that can be printed, λ is the exposure wavelength, and NA is the numerical aperture of the projection lens. The constant k is a dimensionless parameter that is typically in the range of 0.4-0.8. k is decreased by using resist processing tricks and by using optical enhancement with specialized masks. Efforts to improve the resolution capabilities of optical lithography have developed tools that use exposure light with shorter wavelengths. Advances in optical lithography have enabled the tools to reliably pattern circuits with minimum feature sizes of 130nm. Unfortunately, the tool costs for the technologies being developed are expensive (>\$20 M) and have been exponentially increasing with time (see Figure 1.1) [SEMATECH 2000].

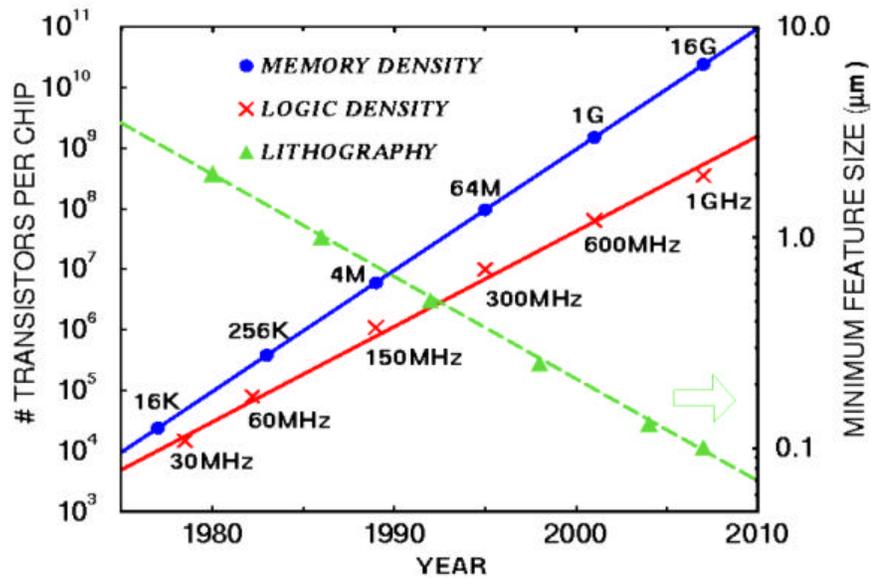


Figure 1.1. Historical data for the number of transistors per chip and minimum feature size for lithography, logic density, and memory density.

The high costs of the higher resolution systems have motivated researchers to investigate new technologies that transfer the high resolution patterns that can be generated by EBEAM lithography without projection optics. Imprint lithography (IL) techniques use templates that are patterned by EBEAM lithography in a molding process. The resolution of IL appears to be limited only by the feature size made on the templates [Colburn, Grot et al. 2001], [Haisma et al. 1996], and [Patterson et al. 1998]. IL processes have the potential for low-cost, high-speed, and high-resolution pattern replication. S-FIL is a novel IL that uses a transparent template that imprints at room temperature and low pressure. This process appears to be better suited for the overlay alignment needed in device fabrication. S-FIL is currently being developed by researchers at The

University of Texas at Austin in collaboration between the departments of Mechanical Engineering (Principal Investigator: Dr. S. V. Sreenivasan) and Chemical Engineering (Principal Investigator: Dr. C. Grant Willson). The S-FIL research group is also working with the Si-Ge-C UHVCVD process group of The University of Texas at Austin department of Electrical Engineering (Principal Investigator: Dr. S. K. Banerjee) in the Microelectronics and Engineering Research Center (MERC) on the Si-Ge-C MOSFET Process Development project. The goal of the work described in this thesis was to develop a basic approach for the integration of S-FIL into a Si-Ge-C MOSFET fabrication process.

1.2 STEP AND FLASH IMPRINT LITHOGRAPHY (S-FIL)

S-FIL is a low pressure and room temperature micro-molding process that uses UV light to cure a liquid monomer solution after it fills the gap between a fused silica (also called quartz) template and the substrate. Figure (1.2) illustrates the flow of the SFILTM process. The quartz template is made from a standard 0.25” thick photolithography mask blank, which is diced to make 1” x 1” templates. The pattern to be molded is patterned onto the quartz with EBEAM lithography, and etched into the quartz a depth based on the desired SFILTM feature height. After the etching the quartz is stripped bare and surface treated with a fluorocarbon self-assembling monolayer (SAM) [Bailey et al. 2000]. The SAM reduces the surface energy of the template, which allows the selective release of the template from the cast imprint. The substrate to be imprinted upon

is covered with an organic “transfer layer”. Core to S-FIL technology is a UV-curing organosilicon monomer solution. This solution is referred to as the “etch barrier”, because it forms silicon dioxide when it is exposed to oxygen, and can be used as a hard mask to etch organics. The etch barrier is dispensed between the mold and the substrate, and as the template nears the substrate the monomer fills the gap and all of the features in the template. After the gap is closed the template can be aligned to the substrate. The template is transparent, allowing alignment between features on the substrate with the features on the template. After the template is aligned, the template is blanket exposed with UV light, which cures the monomer solution. Next the template is pulled away from the substrate, leaving the aligned imprint on top of the planarization layer. The SFILTM process is completed by two etch processes. A halogen etch is used to remove the residual layer of the imprint (Figure 1.2 shows the etch barrier residual layer). The imprinted features mask the organic planarization layer during the oxygen etch. A detailed discussion of the S-FIL process, including its sub-100 nm resolution capability, its ability to self-align, its ability to self-clean (in-situ cleaning of contaminants from the template), and its ability to print over non-flat surfaces is provided elsewhere [Colburn et al. 2001], [Nguyen 2001], [Colburn 2001], [Colburn et al. 2000], [Bailey et al. 2000], [Resnick et al. 2002].

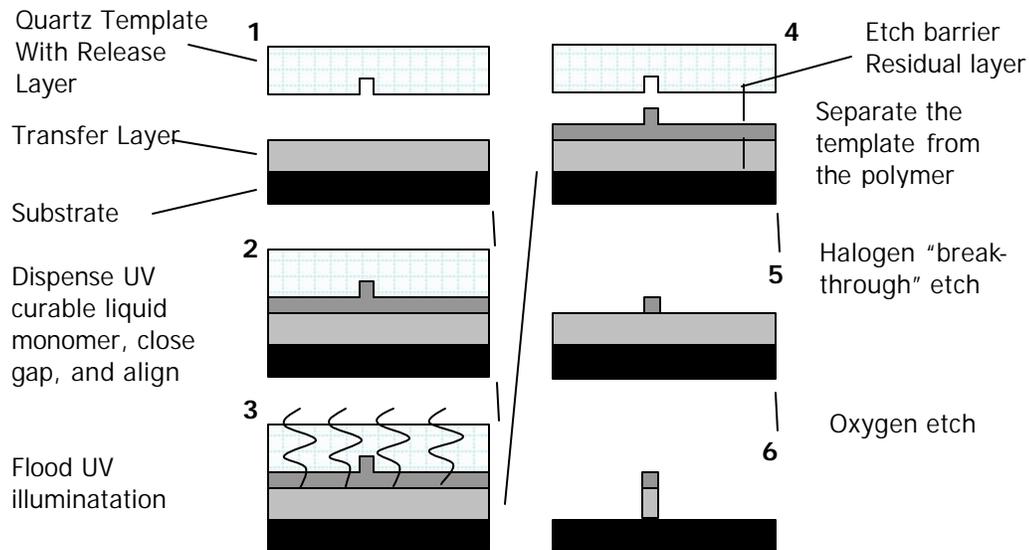


Figure 1.2. The Step and Flash Imprint Lithography process.

S-FIL is capable of layer-to-layer alignment because it is a low temperature and pressure process, which minimizes magnification and distortion errors. The transparent template allows direct inspection of the features on the template and the substrate for optical alignment. After the monomer solution has filled the gap between the template and the substrate, the monomer solution acts as a lubricating layer, allowing smooth, dampened movement [Nguyen 2001] and [Choi et al. 2001]. Sub-micron alignment has been demonstrated previously for S-FIL [Choi et al. 2001].

1.3 Si-Ge-C MOSFET PROCESS DEVELOPMENT PROJECT

The Si-Ge-C MOSFET process is being developed at the Microelectronics Research Center (MRC) at The University of Texas at Austin. This section

discusses the motivation for the project, an overview of existing MOSFET processing and capabilities, and the Si-Ge-C MOSFET process design. A MOSFET fabrication process flow is detailed by Plummer *et al.* 2000. A summary of a Si-Ge-C MOSFET fabrication process flow is given in Section 1.3.2.

1.3.1 Motivation for Si-Ge-C and S-FIL (This section is adapted from Onsongo, 2001)

The motivation for the project is to investigate device scaling and electron mobility in Si-Ge-C. The driving motivations for device scaling are speed improvement, reduced power consumption, and to have a higher device density on a chip [Ng 1995]. Lithographic limitations place a large obstacle on device scaling. The search for answers leads to the investigation of both substrate engineering (higher electron mobility substrates) and new lithography techniques (EBEAM and S-FIL).

In a MOSFET, drive current is the current that flows beneath the gate, between the source and the drain as voltage is applied to the gate and the drain (see Figure 1.3). “IV” curves are plots of the current flow for different constant gate voltages, as the drain voltage is increased. Drive current is one of the dominant parameters in MOSFET performance that affects switching speed and overall system performance [Streetman, 1995]. In an effort to get higher drive currents, MOSFETs are made with shorter gate lengths and higher electron mobility. Figure 1.3 shows both top and cross-sectional views (not to scale) of the Si-Ge-C MOSFET design. Si-Ge-C MOSFETs have been shown to have

higher drive current than traditional Si MOSFETs [Onsongo 2001]. A PMOS comparison for gate length = 0.1 micron and width = 3 micron shows $\text{Si}_{0.795}\text{-Ge}_{0.2}\text{-C}_{0.005}$ samples having a 14% drive current enhancement over equivalent epitaxially grown Si. Our goal here was to establish a process for aligning and patterning the gate structure in the device.

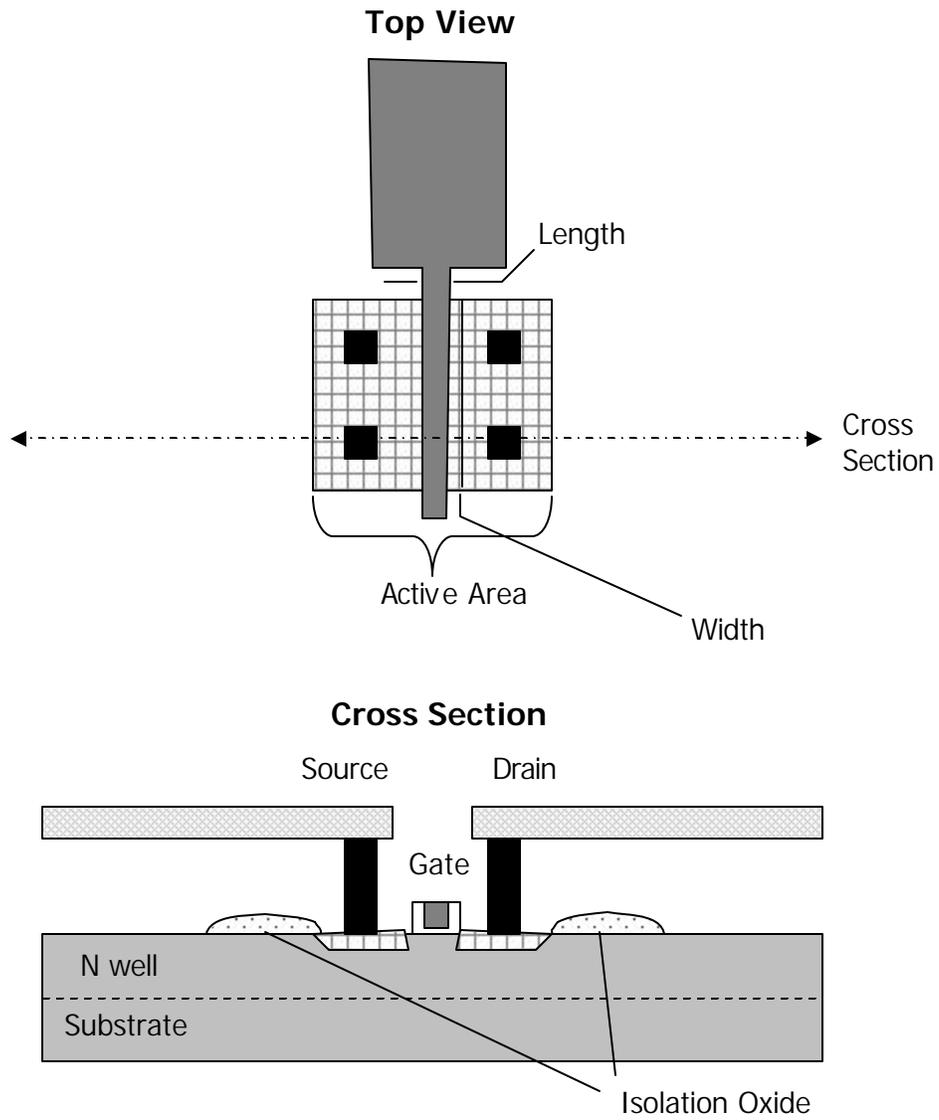


Figure 1.3. Si-Ge-C MOSFET Design.

Currently, high resolution EBEAM lithography is used to make the Si-Ge-C MOSFETs. EBEAM lithography has significant advantages for this project development. It is an established technology with pattern placement precision and high resolution (50 nm) pattern capability. It allows for flexible experiment

design implementation. Also, high-aspect-ratio POLY patterning and etch are well established techniques. The disadvantages of EBEAM lithography in general are mainly the time, cost, and trouble with topography.

1.3.2 Si-Ge-C MOSFET Fabrication Process

The Si-Ge-C MOSFET project fabrication process flow is shown in Figure 1.3. The schematics represent cross-sections similar to the one shown in the previous figure, and are not to scale for clarity. The process begins with a silicon wafer. The epitaxial Si-Ge-C channel and Si cap are grown via ultra-high-vacuum chemical vapor deposition (UHVCVD). Next low-temperature oxide (LTO) is deposited by chemical vapor deposition (CVD). Low-resolution contact (optical) lithography is used to define the ACTIVE pattern. After the etching of the isolation oxide with the ACTIVE pattern, the gate oxide is grown. Poly-Si (Poly) is then deposited via low-pressure chemical vapor deposition (LPCVD), and a 50 nm oxide hard mask is deposited directly afterwards. The hard mask is used to ensure good etch selectivity and to avoid contaminating the Si etching chamber. Next either EBEAM or S-FIL is used to pattern the high-resolution POLY (gate structure) pattern. This pattern is transferred through the hard mask and the Poly with reactive-ion etching (RIE). This step is followed by the ion-implantation of the source, drain, and gate, and the deposition and etching of the spacer oxide around the gate. To electrically isolate the gate and active area, more oxide is deposited and patterned using a low-resolution CONTACT pattern, which makes paths for the metal contacts to reach the source, drain, and gate. The

process is completed after Al is sputtered, patterned with the low-resolution METAL pattern, and etched, leaving the large metal contacts exposed on the surface of the finished wafer.

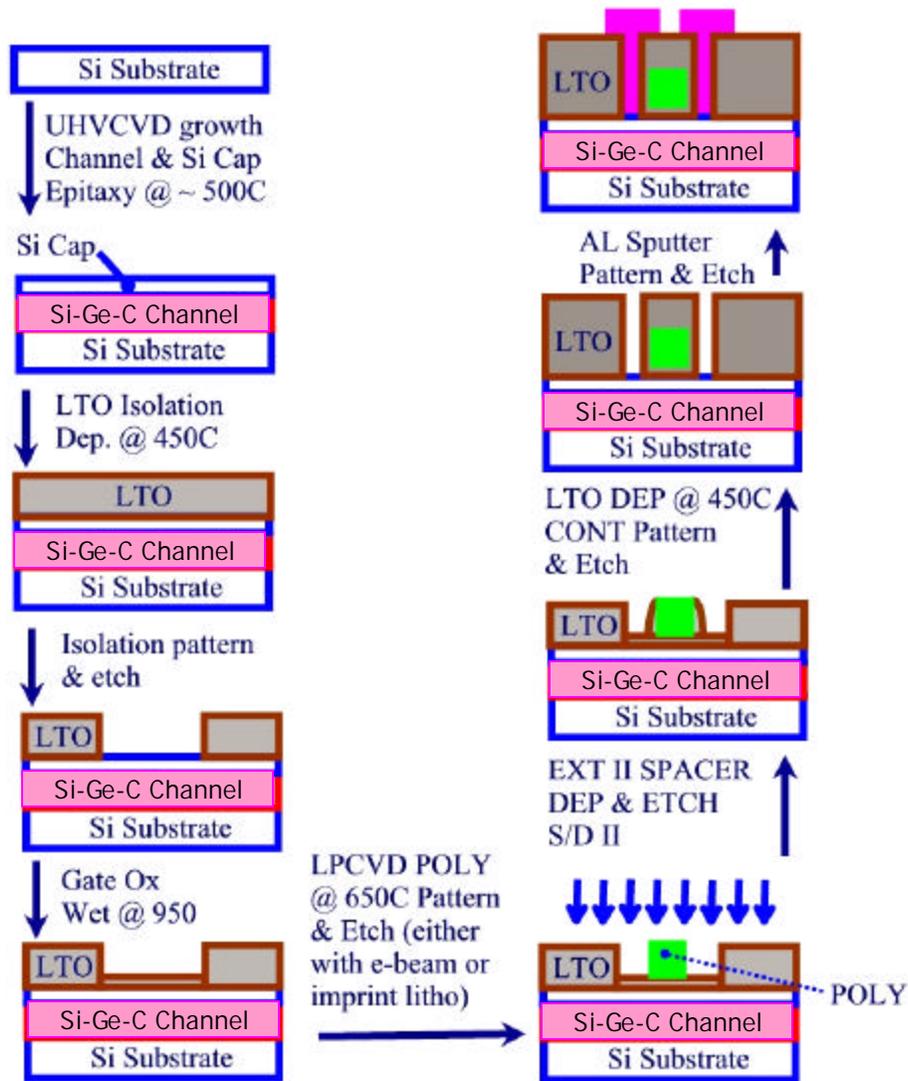


Figure 1.4. Si-Ge-C MOSFET Fabrication Process Flow.

1.3.3 ACTIVE Patterned Topography

The first significant topography on the wafer is produced when the LTO isolation oxide layer is etched to produce the ACTIVE pattern. The height of the topography is principally determined by the thickness of the oxide layer that was deposited. To minimize the planarization needed, the oxide layer is deposited at the minimum allowed thickness for the device of 250 nm +/-20 nm. Although layers of Poly and oxide are deposited on top of the topography, the effective height of the topography remains the same because these CVD processes are very conforming. The transitions of the topography at the edges of the features are defined by the wet-etch processes, and are about 50-60 degrees. This slope is beneficial to the processing, as it allows good continuity of deposited films. Figure 1.5 shows a scanning electron micrograph (SEM) of a cross-section of a wafer that has the ACTIVE pattern wet-etched into the oxide, with Poly and oxide deposited on top. The approximate film thicknesses are 250nm, 140nm, and 50nm respectively. The left side of the image is higher than the right because the original oxide layer that was on the right side was etched away. The sample is viewed with a tilted orientation, held at 60 degrees away from the horizontal plane (30 degrees from a true cross-sectional view). The roughness of the films is mostly caused by excess Au-Pd coating for the SEM imaging.



Figure 1.5. SEM image of cross-section wall slope to ACTIVE pattern area.

1.3.4 ACTIVE and POLY Patterns

The MOSFET process described is performed on 4" wafers. The low resolution lithography steps are performed with a Karl-Suss contact printer. The lithography masks were designed with layout shown in Figure 1.6. The masks contain features that allow the fabrication of a variety of features, including MOSFETS, resistors, capacitors, and alignment marks. The fabrication of the MOSFETS is the subject of this thesis, and all other features will not be discussed in detail, except features that will be used to measure planarization and alignment accuracy. The alignment marks will be discussed in Chapter 3. The patterns are organized in an arrangement that make up one die, which is about 6 mm wide by

9 mm long. More than one die will be referred to as “dies”, for distinction from the word dice that will be used to refer to the cutting of wafers. The dies are arranged in rows, similarly to the pattern shown in the schematic in Figure 1.6. Also shown in Figure 1.6 is the orientation of the dies on the wafer. Although the placement is symmetric, all the dies are oriented in the same direction. Specifically the high resolution gate structures (50 to 800 nm) are all on the same side of dies. Also shown in the figure are the locations of the rows of MOSFETs on the die.

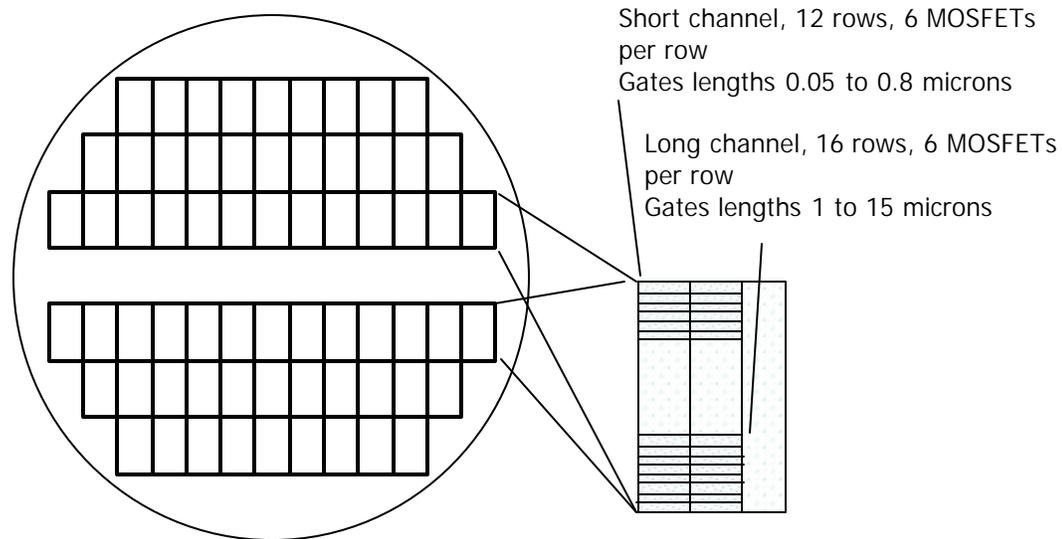


Figure 1.6. Schematic of a 4” wafer showing the placement of dies of the lithography patterns, the orientation of the dies, and the position of the rows of MOSFETS.

In order to study the effect of the gate dimensions on drive current, the masks used in the Si-Ge-C fabrication process include arrays of MOSFETs with varying gate width and lengths. On each die, there are 28 rows of MOSFETs.

Each row has six MOSFETs; all with the same gate length but varying gate widths (3, 5, 8, 13, 18, and 23 microns). There are rows of MOSFETs with gate lengths equal to 0.05, 0.10, 0.15, 0.20, 0.25, 0.30, 0.40, 0.50, 0.60, 0.70, 0.80, 1, 2, 3, 4, 6, 8, 10, and 15 microns. The arrangement of the different MOSFETs is described in Chapter 3. The S-FIL templates for this work were made by Motorola Labs (Tempe, AZ).

Figure 1.7 shows a schematic of a die, showing the arrangement of the rows of MOSFETs on a die. Each row is labeled with a letter and a number. Each row of MOSFETs on the POLY pattern is labeled. The last letter of the label designates each row; only the last letters are shown for clarity. The number in each row corresponds to the designed gate lengths of the MOSFETs in the row (see Figure 1.3 for definitions of gate length and width).

	T, 0.80	N, 0.30
	S, 0.70	M, 0.25
	R, 0.60	L, 0.20
	Q, 0.50	K, 0.15
	P, 0.40	J, 0.10
	O, 0.35	I, 0.05
	H, 15	H, 15
	G, 10	G, 10
	F, 8	F, 8
	E, 6	E, 6
	D, 4	D, 4
	C, 3	C, 3
	B, 2	B, 2
	A, 1	A, 1

Figure 1.7. Schematic showing the arrangement of the rows of MOSFET on a die, with their respective gate lengths.

Figure 1.8 shows optical images of a row of the ACTIVE pattern (upper), and a row of the POLY pattern (lower). The row of the ACTIVE pattern shows 6 sets of features, each with a different sized active area ranging from 3 to 23 microns (from left to right). Figure 1.9 shows SEM images showing the range of sizes of areas to be planarized on the ACTIVE pattern. The left and right images are for MOSFETs with 23 and 3 micron gates widths, respectively. The gate lengths are determined by the vertical (with respect to this page) dimension of the

center feature (of the three) for each MOSFET active area seen in Figure 1.9 and the upper images of Figure 1.8. The two high-aspect ratio rectangles in each image in Figure 1.9 and in the upper images of Figure 1.8 are for use in CMOS applications and are not of interest for this thesis. Figure 1.9 is a top-down SEM image that shows a closer look of part of a MOSFET gate structure from the POLY pattern.

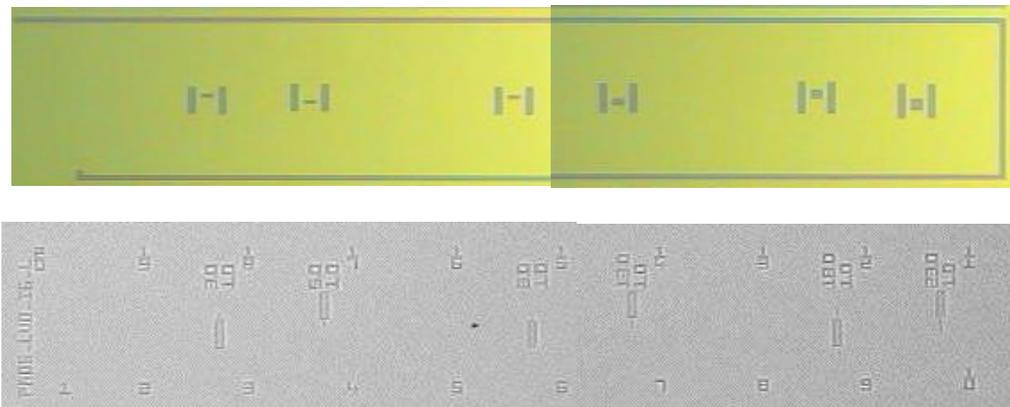


Figure 1.8. Optical Images showing a row of the ACTIVE pattern (upper) and a row of the POLY pattern (lower).

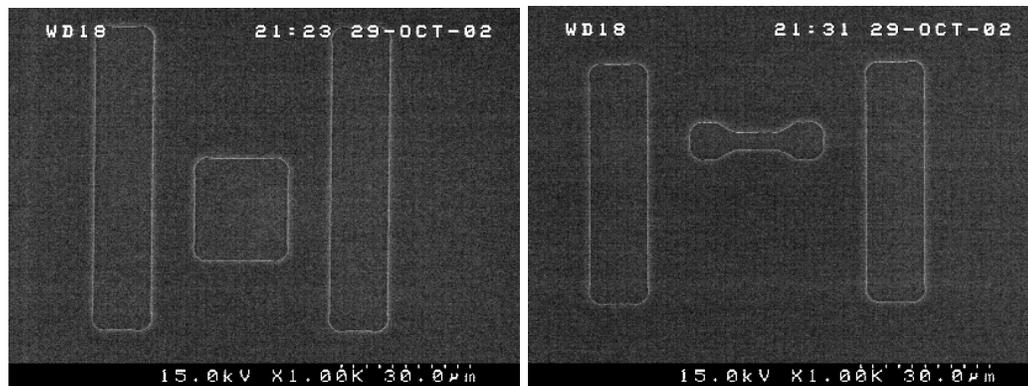


Figure 1.9. Top-down SEM images showing the range of sizes of areas to be planarized on the ACTIVE pattern. The left and right images are for MOSFET with 23 and 3 micron gates widths, respectively.

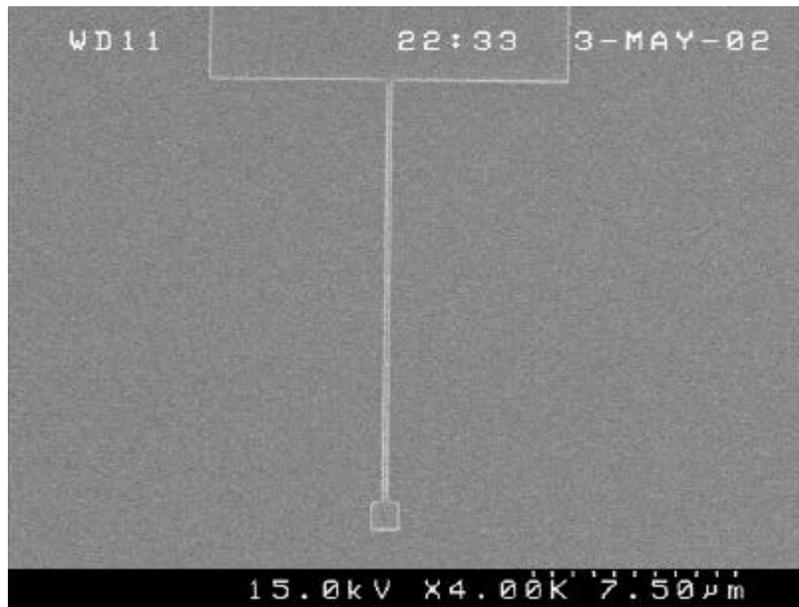


Figure 1.10. Image showing a closer view of part of a MOSFET gate structure.

1.4 THESIS OVERVIEW

In this thesis, S-FIL will be used in the MOSFET fabrication process to define the POLY (gate structure) pattern. The processing included with the S-FIL can be lumped into three steps: planarization, imprinting and alignment, and etching (see Figure 1.4). The topography defined by the ACTIVE pattern needs to be planarized so that the imprint can be properly transferred by the etching step. The imprint and alignment of the POLY pattern will be done with the S-FIL overlay alignment machine described in Chapter 3. The imprinted POLY pattern needs to be transferred through the planarization layer by reactive-ion etching. This is done with two etching steps – the first to remove the residual layer of the S-FIL imprint and the second to transfer the pattern through the planarization

layer. At the end of this step, an etch mask that can pattern the oxide is established. This is equivalent to the completion of an optical lithography process at the end of the resist development step.

The planarization layer is used to mask the oxide hard mask. After an organic strip/clean, the oxide hard mask can then be used during the etching of the Poly. It is a requirement of the planarization layer to function as a mask for the etching of the hard mask, but the etching of a thin oxide hard mask with an organic resist, and the subsequent Poly etch are established processes and are not in the scope of this thesis.

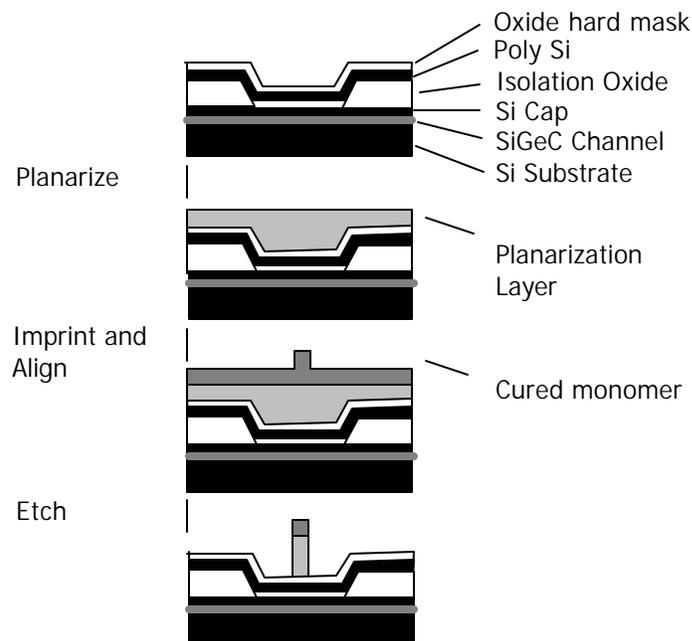


Figure 1.11. S-FIL Processes for Integration into Si-Ge-C MOSFET Fabrication Process.

The goals of this thesis are:

- ? Define the engineering requirements of the planarization layer

- ? Evaluate different methods for planarization
- ? Demonstrate a process for alignment and imprinting the POLY pattern over a planarized ACTIVE pattern
- ? Characterize the etching processes specific to the S-FIL processing
- ? Develop a strategy for etching based on the planarization and imprinting achieved

For S-FIL to become a practical technology, processes for its implementation in device fabrication must be developed. The important issues associated with the planarization needed, the alignment and imprinting performed, and the etching to be done (based on the imprint and planarization achieved) are discussed. The remainder of this thesis has been organized into 4 chapters. Chapter 2 discusses the planarization needed for the S-FIL, planarization theory, and the results of experiments determining the feasibility of different methods. Chapter 3 discusses the imprinting and alignment process. Information about the S-FIL Overlay and Alignment Machine is provided, and the results of the alignment and imprinting of the POLY (gate) pattern on the planarized ACTIVE pattern are discussed. Chapter 4 presents the etching needed for the Poly (gate) pattern transfer. Chapter 4 includes experimental results of the etching processes, and problems encountered with the etching processes. Strategies for determining etching times and predicted the device yield to expect given the process conditions achieved. Chapter 5 summarizes this research and suggests future work for the of integrating the S-FIL processing in device fabrication.

Chapter 2: Planarization

2.1 INTRODUCTION

This chapter contains the development of a basic approach for the planarization needed for the integration of S-FIL in the Si-Ge-C MOSFET fabrication process. The first section of the chapter explains the needs for planarization for the S-FIL process. From these needs, the requirements and specifications are explained and summarized in a chart. Planarization alternatives are explained, and their potential feasibilities are discussed. Finally, experiments to determine the planarization achieved by different methods are presented and discussed.

2.2 NEED FOR PLANARIZATION FOR S-FIL INTEGRATION INTO MOSFET FABRICATION PROCESS

In previous publications, the S-FIL process has been shown to require a “transfer layer” below the S-FIL imprint. This layer is normally spin-coated onto a flat wafer. This layer is needed to ensure adhesion of the imprint, to create high aspect ratio features, and to act as a resist for pattern transfer. The need for the planarization layer as described in this thesis combines the needs of a transfer layer and the need for planarization. Planarization is needed for patterned feature preservation across the topography, and to minimize the burden on the break-through halogen etch.

In order to explain the needs for planarization, some fundamentals of the break-through etch should be explained. The break-through etch determines what

pattern will be transferred through the planarization layer and ultimately through the Poly. Whatever imprinted material is present after the break-through etch will mask the underlying transfer layer in the oxygen etch. The etching process can be discussed in terms of the time that the material was etched or depth of material removed. Although the etch rate may not precisely be constant with respect to time, for this analysis it is assumed so.

For example, in order to remove the residual layer, the break-through etch must be long enough to remove all of the imprinted residual layer. This can be stated as either etching for a time, or simply a depth. If the break-through etch is not long enough, then the residual layer will not be completely removed. If the break-through etch is too long, the imprinted feature may be partially (or completely) removed by the etch.

2.2.1 Minimize the Break-through Etch

To minimize loss of features, the break-through etch should be minimized, and the underlying residual layers should be uniform in thickness. The duration of the break-through etch must be sufficient to remove the maximum thickness of the residual layer. The minimum residual layer thickness will then be overetched with potential loss of features and CD (if the etch process is not anisotropic). The anisotropy of the etch processes are defined by the vertical etch rate divided by the horizontal etch rate. All of the etch processes shown in the figures in this thesis are shown to be highly anisotropic – the feature widths do not change from result of the etch process. Although the etcher used for this project does not etch

with perfect anisotropy, for this analysis the etching processes used are assumed to be anisotropic.

With good planarization, the minimum time for the break-through etch is only determined by the residual layer thickness of the imprint. Figure 2.1 shows why planarization minimizes the break-through etch. There are schematics of cross-sections (not to scale) of two series of processing shown, one with bad planarization and one with good. Part of the imprinted feature is above the depression in the topography and part of the imprinted feature is outside of the topography. The features do not represent mis-aligned gate structures. There are three processes shown in each series - planarization, imprint and align, and anisotropic break-through etch. The black layers represent the substrate with topography to be planarized, the light grey layers represent the planarization layer, and the dark grey layers represent an aligned imprint. The upper series of processes shows the effect of good planarization. The residual layer is thin and uniform, and the break-through etch is short. The lower series of processes shows the effect of bad planarization. The residual layer is thicker in the trench than outside of the trench, because of the depth of the depression in the surface of the conforming planarization layer. In order to remove the residual layer at the bottom of the depression trench (and to cleanly transfer the part of the feature in the depression), the break-through etch must be long enough to etch the thickness of the residual layer plus the depth of the depression in the surface of the planarization. Note that in both of these cases the imprinted features are

transferred as desired, but the feature imprinted over the bad planarization needed to be etched longer.

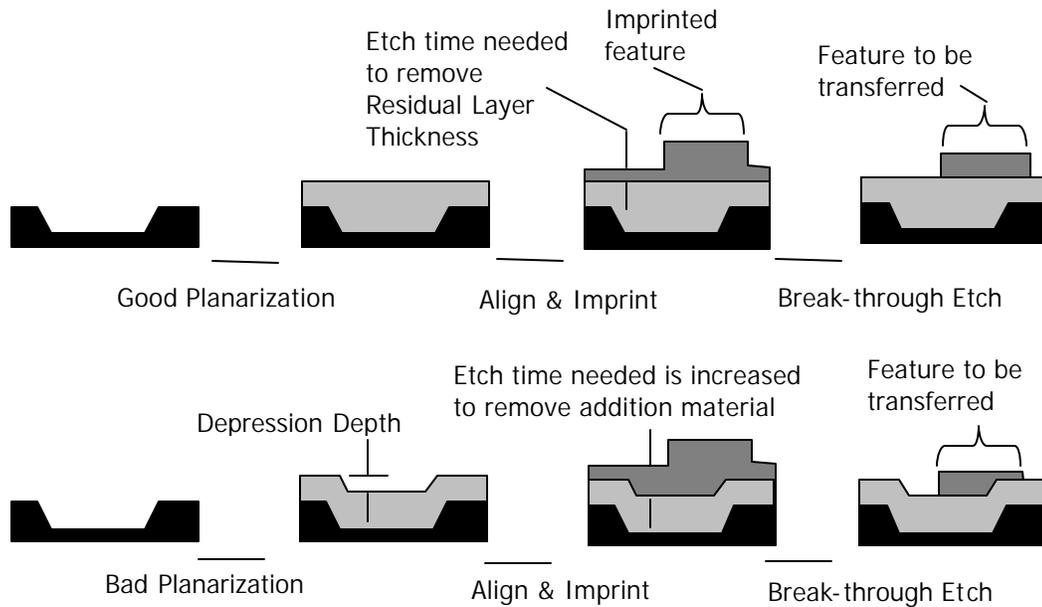
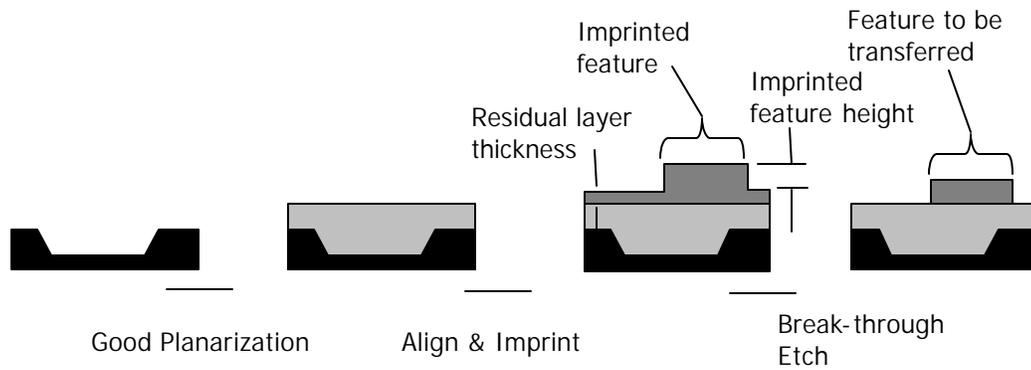


Figure 2.1. Planarization is desired for minimizing the break-through etch.

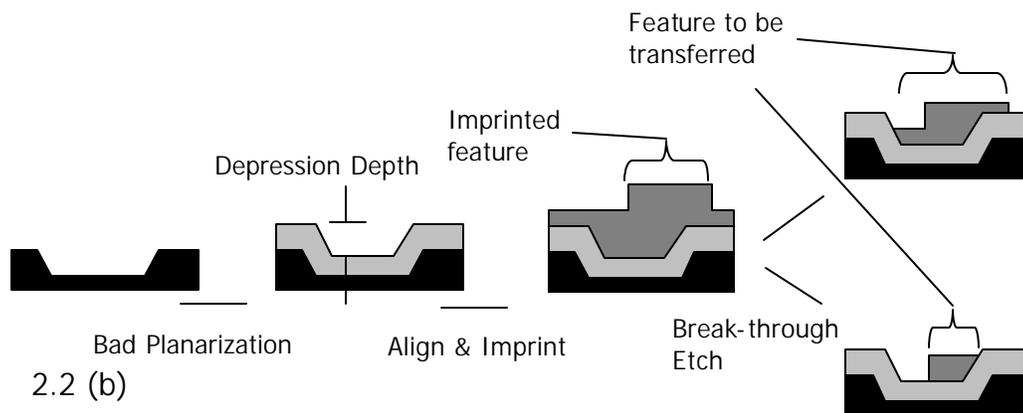
2.2.2 Feature Preservation Over Topography

Although S-FIL can tolerate some variation in residual layer thickness, too much variation will disturb the pattern transfer, and either cause undesirable masking or incomplete pattern transfer. Figure 2.2 shows why planarization is needed for imprint feature preservation across topography. There are schematics of cross-sections (not to scale) of two series of processing shown, one with bad planarization and one with good (Figures 2.2(b) and 2.2(a), respectively). Part of the imprinted feature is above the depression in the topography and part of the imprinted feature is outside of the topography. The features do not represent mis-

aligned gate structures. There are three processes shown in each series - planarization, imprint and align, and anisotropic break-through etch. The black layers represent the substrate with topography to be planarized, the light grey layers represent the planarization layer, and the dark grey layers represent an aligned imprint. The series of Figure 2.2(a) shows the effect of good planarization. The residual layer of the aligned imprint has uniform thickness over the topography. The break-through etch is only needed for the depth of the residual layer at the top of the step, and the entire feature is transferred. The series of Figure 2.2(b) shows the effect of bad planarization. The planarization layer conforms to the topography of the substrate. The thickness of the residual layer of the aligned imprint varies by the amount of the flatness of the surface of the planarization layer. The break-through etch must be long enough to remove the thickest part of the residual layer. The break-through etch will be longer than necessary for the features out of the trench, in order to completely remove the residual layer in the bottom of the trench. If the depth of the topography is greater than the feature height, then all of the features cannot be transferred. The two cases for the break-through etch are shown. Either the features out of the depression will be etched completely away (lower case of Figure 2.2(b)), or some of the residual layer of the imprint will remain in the bottom of the trench and undesirably mask the underlying layers (upper case of Figure 2.2(b)). The allowable variation in the flatness of the surface of the planarization layer is discussed in more detail in the following section.



2.2 (a)



2.2 (b)

Figure 2.2. Planarization is needed for feature preservation over topography.

2.3 REQUIREMENTS FOR PLANARIZATION

In this section the requirements of the planarization layer are discussed and summarized in a list. Their definition and their realization are the goals of the planarization part of the project. The requirements for the planarization layer to transfer the POLY pattern are assumed to be:

- ? Planarize the Area of one MOSFET (approximately 100 ? m x 100 ? m)

- ? Planarize the largest active area (25 μ m wide, 250 nm deep trenches) with maximum flatness (over the ACTIVE pattern) over the area of the MOSFET to lead to acceptable residual layer thickness variation
- ? Maximum thickness (1 μ m)
- ? Minimum thickness (50 nm)
- ? Low contaminants, voids, and defects to achieve a working MOSFET
- ? Thickness can be measured accurately to allow for etch calibration
- ? Be readily etched in an O₂ plasma
- ? Good adhesion to the imprint and the oxide
- ? Not mix with or swell when in contact with the etch barrier during imprinting

The above requirements are discussed in more detail in the following paragraphs.

2.3.1 Planarize the Area of One MOSFET

The area of the wafer that needs to be planarized is the area underneath the imprinting template. Colburn et al. (2001) have demonstrated planarization for imprint lithography as discussed in section 2.4.

Because the current S-FIL overlay alignment machine (OAM) only imprints in the center of the wafer, only that region needs to be planarized. If the planarization was done in a manner that created a uniform thickness, over a greater area than the area imprinted upon, this would allow for easy measurement of the planarization thickness. For proof of concept, the minimal area needed to be planarized is the area used to make one MOSFET. This area is defined by the active area and the area including the gate structure. This field is less than 100 microns x 100 microns. Although minimally one MOSFET would be proof of

concept, to get statistically significant data for the Si-Ge-C MOSFET project, dozens of working MOSFETs are desired.

2.3.2 Planarize the Largest Active Area

The topology to be planarized is the active areas. As mentioned in Section 1.3.3, the topology depth is determined by the isolation oxide thickness and its minimum value is 250nm \pm 20nm. The variation is wafer to wafer and is caused by the oxidation batch processing. The variation across the center 1" of the wafer is negligible for the purposes of this thesis. As shown in Figure 1.9, the active areas vary in length and width. The requirement of the planarization is to planarize the largest active area, which is approximately 23 μ m by 21 μ m.

2.3.3. Maximum and Minimum Thickness

One important requirement of the planarization layer is the maximum thickness. After the break-through etch, the imprinted POLY pattern is transferred through the planarization layer by an oxygen etch. When masked with SiO₂, organic layers can be etched nearly anisotropically. Anisotropy can be defined as the vertical etch rate of a material divided by the horizontal etch rate. Very high anisotropy has been reported while oxygen etching organics [Colburn 2001]. The etcher being used at the MRC facility has etched with Anisotropy of greater than 20 (see Chapter 4). There is not a specification for CD loss on the Si-Ge-C gates, although, the CD loss should be minimized.

The factors that affect the maximum thickness decision include etch selectivity of etch barrier with respect to the transfer layer, and the maximum allowable CD loss. Due to the low anisotropy of the etcher used, this thickness was not fully optimized during this work. For the purposes of the reported experiments, a maximum thickness of 1 micron was assumed.

A minimal thickness of planarization material is required to act as a mask for the etching of the oxide hard mask. The thickness required depends on the selectivity of the oxide etching process. The selectivity is defined as the etch rate of material A divided by the etch rate of material B. The selectivity for organic films to oxide is approximately one. For an oxide hard mask that is approximately 50 nm thick, the minimum thickness of the planarization layer is approximately 50 nm.

2.3.4 Contamination Issues

An important requirement of the planarization layer is that it must be free of contaminants and particulate defects. Due to the small scale and nature of the devices, only semiconductor grade materials were used. All processes must leave the surface particulate free to provide a high yield of MOSFETs.

2.3.5 Thickness Can Be Measured Accurately

The thickness of the planarization layer must be measurable. The etching system at the MRC does not have end-point detection so there is no way to know when the etching of each layer has broken through to the layer below. For this

reason, the time of etch is calculated by assuming the etch rate, and measuring the thickness of the layers to be etched. There are a few ways to approximate the thickness of the planarization layer in the region that will be imprinted, but there is a constraint on the measurement. The region of the wafer that is going to be imprinted upon cannot undergo destructive testing. The area can be measured by non-destructive means, such as ellipsometry – but cannot be measured by a profilometer. If the planarization layer has uniform or a predictable thickness, the thickness can be approximated by measuring the thickness of the planarization outside of the imprinting area. Another alternative for the thickness measurement is to dice the wafer after the patterned imprint, and look at the cross-section with an SEM. The different layers should be visible after a short “decoration” oxygen etch, which would partially etch the organic planarization layer. Although this method is destructive, it is viable for this project because pieces of wafers can be processed.

2.3.6 Be Readily Etched in O₂ Plasma

The planarization material must consist of organic compounds that do not contain elements that form refractory oxides, so that it can function in the etching processes. The organosilicon etch barrier forms silicon dioxide when it is exposed to an oxygen plasma, and has high etch resistance to oxygen etching thereafter. The planarization layer must be readily etched in the oxygen etch, but slowly etched in halogen RIE, because the planarization layer also must act as a

resist for the etching of the oxide hard mask. There are well established processes for etching SiO₂ with organic resists.

2.3.7 Good Adhesion

The planarization material must have good adhesion to both the oxide hard mask, and to the patterning imprint. The adhesion of the planarization to these layers will be stressed during the separation process of the imprinting, and during the etching processes. During the separation process of imprinting, selective adhesion is needed to separate the imprinting templates from the cured etch barrier, while the etch barrier remains attached to the transfer layer. This ensures that the imprint is anchored to the planarization layer, and the planarization layer to the substrate. In this case, the low surface energy of the template causes the imprint to separate from the template every time. If the planarization layer has poor adhesion to the oxide, the imprint may not separate from the template.

2.3.8 Not Mix with the Etch Barrier

The planarization layer must not mix with the etch barrier monomer solution during the imprinting process. The etch barrier will be in contact with the planarization layer during the imprinting process, and during alignment. Many factors contribute to the chemical resistance of the films, and the compatibility should be determined experimentally. The planarization layer is less likely to swell upon contact with the monomer solution if it is heavily cross-linked.

2.3.9 Four-Inch Wafers

The planarization process must be carried out on four-inch wafers because the tools used in the fabrication process at the MER are all designed to process four-inch wafers.

2.3.10 Flatness Variation

Thick, stable templates are used in the S-FIL process. Over the region of interest, unetched portions of these templates are assumed to be optical flats. The inherent purpose of a planarization layer is to cover the topography and present a planar surface with significantly less topography. This section defines the requirement of the minimum allowed flatness in the top surface of the planarization layer. The flatness after planarization must be significantly less than the imprinted feature height, but additional factors influence the variation budget. Figure 2.3 shows a schematic used to determine the flatness requirement and define the terms to be used in this discussion.

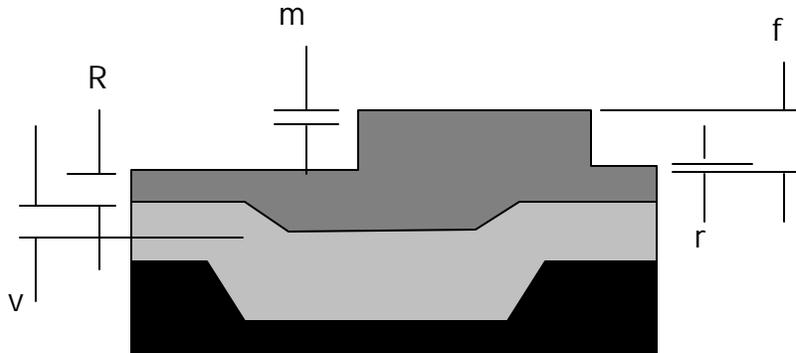


Figure 2.3. Schematic showing imprint on planarization layer, used to determine variation in flatness requirement and define terms.

The three layers in the diagram are the substrate (black), planarization layer (light grey), and patterned imprint (dark grey). There is topography shown in all of these layers, and each is different. The topography shown in the substrate represents the active area pattern. This defines the bottom surface of the planarization layer. The top surface of the planarization layer has a depression shown. This surface determines the bottom surface of the patterned imprint. The magnitude depression in the top surface of the planarization layer is defined as 'v'. The top surface of the patterned imprint has the topography formed by the relief on the S-FIL template, and is referred to as a feature. The height of the feature on the imprint is defined as 'f'. The thickness of the residual layer of the imprint is defined as 'R', although this term is also defined as the vertical distance etched by the break-through etch. Figure 2.3 shows the three layers before any etching, although some of the terms defined are significant only after etching. The terms 'm' and 'r' are influenced by roughness in the surface produced by the

RIE process. This roughness is bad for the pattern transfer because additional etching is required to remove undesired etch barrier material left on the etched surface after the theoretical minimum etch was performed (assuming no roughness and no over-etching). The peak-to-peak roughness of the etched surface of the imprint after the required break-through etch is defined as 'r'. This term 'r' also represents the minimal amount of over-etching needed for good pattern transfer. The roughness on top of the feature to act as a mask is unfavorable, because the low spots in the mask could cause pitting or "pin-holes" in the feature if a minimal thickness of the mask was used. The peak-to-peak roughness of the top surface of the imprint plus the minimal thickness of etch barrier that is required to act as a mask for the etching of the planarization layer is defined as 'm'.

The minimal amount of over-etching needed can be approximated by the roughness height of the break-through etched surface. Figure 2.4 shows a circular tower feature that was imprinted and then halogen etched. The approximate roughness of the surface away from the feature is 20 nm. The roughness of the top of the feature is harder to estimate because of the "crown" effect created by the deposition of material on the vertical surfaces of the feature. This roughness is significantly greater than 20nm, although the roughness in the center of the feature is approximately 20nm.

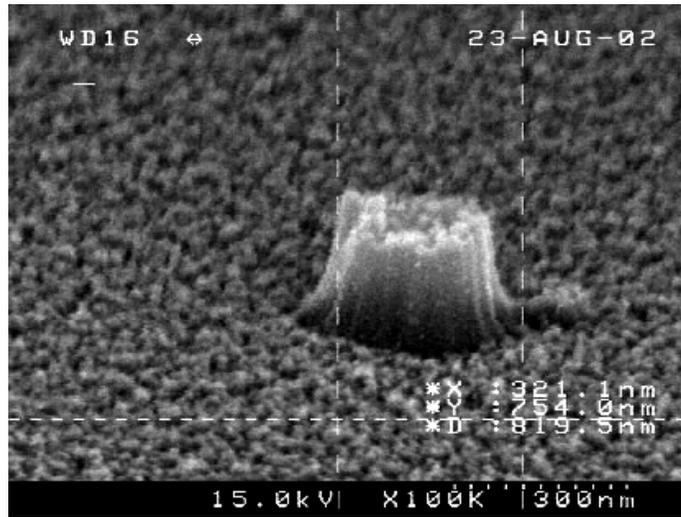


Figure 2.4. Surface after break-through etch shown to document surface roughness.

The minimal thickness of material needed to mask the planarization layer is determined by the thickness of the planarization layer and the etch selectivity of the two materials. Etch selectivity is defined as the (vertical) etch rate of the planarization material divided by the etch rate of the etch barrier (under the same etching conditions). The minimal thickness to mask is

$$mask_thickness_{min} = \frac{planarization_thickness}{etch_selectivity}$$

The etch selectivity of organic resists to the etch barrier varies with the planarization material chosen, the exact etching conditions, and the Si content of the etch barrier. The etch barrier formulation used in this study has a Si content of approximately 12 % by weight. The etch selectivity between this etch barrier and a polystyrene film has been shown to be around 12 [Colburn, 2001]. The etch rates will vary from etcher to etcher and with set conditions in a given etcher.

Assuming the maximum planarization thickness of 1 micron, and the selectivity of 12, the minimum thickness for a mask is 83 nm. For every 100 nm of additional thickness of the planarization layer, the minimal mask must be about 8.3 nm thicker.

In addition to the previously defined terms, the variation in thickness of the etch barrier imprint residual layer is involved in the determination of the requirement for the planarization. Variation in the thickness of the imprint increases the minimum allowed flatness of the planarization. In order to calculate the requirement, the maximum expected variation in etch barrier residual layer must be estimated. For the minimal requirement of transferring one MOSFET, the variation could be approximated for the area of 100 microns. Even if the large variation over the 1" template is 200nm and symmetric, the variation across the 100 micron field is only

$$R_v \approx \frac{200nm \cdot 100\mu m}{1"} \approx 1nm$$

which is in the noise of all the other approximations. However, the impact of the variation in residual layer becomes more significant as the area desired to be transferred increases, or the variation in residual layer of the imprint increases. The value of R_v will not be included in the requirement for planarization, although the term will be included in the relationship. The relationship of area to be transferred based on variation in residual layer thickness and the flatness of the planarization surface is explored further in Chapter 4.

The template was etched so that the heights of the features on the POLY template are 250nm. This value was chosen because it is the approximate

maximum feature height that can imprint 50 nm wide features (resulting in a relatively aggressive 5:1 aspect ratio imprinting). The feature height of the imprint is less than the height of the template because of the densification of the polymer when it is cured. The vertical shrinkage of the feature height varies with the etch barrier formulation and the line width. For the etch barrier formulation used and a 250 nm wide line, the feature height shrinks vertically by about 7% [Colburn 2001]. This makes the feature height f equal to about 233 nm.

The variations in the etching process also affect the pattern transferred. Time and spatial variation in the etch rates, as well as uncertainties in the film thicknesses and the predicted etch rates are not included in this analysis.

Using the previous terms, the maximum allowable variation in flatness of the planarization layer can be estimated to be:

$$v_{\max} \approx f + r + m + R_v$$

Using values ' f ' = 233nm, ' r ' = 20nm, and ' m ' = 103nm gives the flatness requirement for the planarization is 110nm – ' R_v ', as stated earlier ' R_v ' is the variation in thickness of the etch barrier residual layer, and is neglected for imprints over a small region.

2.4 PLANARIZATION BACKGROUND AND ALTERNATIVES

Planarization is used in the microelectronics world to create a smooth surface over rough topography and to allow a smaller depth of focus for photolithography. The planarized surface aids in continuity of deposited layers, and the smaller depth of focus allows a greater numerical aperture, which then

allows higher resolution patterning [Sheats and Smith, 1998]. In this section, background information on planarization alternatives is given, with some discussion on their feasibility for this project. Spin-coating, spin-coating with reflow, spin-coating with etch-back, chemical-mechanical polishing (CMP), and contact planarization are discussed.

The discussion of planarization is aided by a metric for comparison of alternative processes. A method of characterizing the extent of planarization by simple ratios of planarizing film thicknesses is percent planarization [Stillwagon and Taylor 1989]. Figure 2.5 shows a schematic of an etched trench of depth d in a substrate that has been coated with a planarizing film of thickness h (not to scale). The topography causes a depression in the planarization film of depth d_d , which is related to the degree or percent planarization (100% is perfect planarization). The percent planarization is calculated from

$$\% Planarization = \frac{d - d_d}{d} \times 100$$

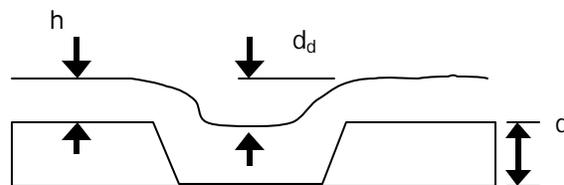


Figure 2.5. Definition of percent planarization.

For the integration of S-FIL into the Si-Ge-C MOSFET fabrication process, the percent planarization needed is determined by the topography height of the ACTIVE pattern (250nm) and the maximum flatness, or depression depth allowed (110nm). The percent planarization needs to be at least 56%.

2.4.1 Spin-Coating

Spin-coating is the industry standard for photolithography planarization. It is a simple, clean, and low-cost process. The spin-coating process begins with a liquid consisting of a solvent and resin that is dispensed onto the wafer. The wafer is then spun at 1000-4000 rpm for about a minute, and then baked. The spinning process spreads the liquid into a thin and uniform film across the wafer. The film is baked to drive out residual solvent, to anneal stresses from the spinning and evaporation processes, and sometimes to cross-link the film.

Perfect planarization cannot be achieved using spin-coating process that uses a resin dissolved in a solvent. The volume change from the evaporation of solvents causes the parts of the film above low-lying features to shrink more than parts of the film above high-lying features.

Of all of the requirements, the measured quantities of the spun film emphasized for feasibility are the final film thickness, and the extent of planarization. Only purely organic, semiconductor grade mixtures were considered, which satisfy the requirements for etching and contamination issues. Spin-coating was done on 4" wafers, and the area planarized is greater than the imprinted area of the wafer. The spin-coating process produced films with thickness variations less than 20nm over the area of the imprint, which would allow measurement of the final film thickness without affecting the imprint. The adhesion of the films to oxide and to the etch barrier can be determined experimentally, and could be improved if necessary by adhesion promoters such as HMDS.

The thickness of the spun films and the extent of planarization by spin-coating are dependant upon material properties of the liquid, spin-coating parameters, and the substrate topography. Important properties of the liquid include polymer molecular weight, solids content, and solvent type. Influential spin-coating parameters are coating speed, acceleration, time, temperature, and exhaust. The substrate topology height, width, shape, orientation, and pattern density all determine the extent of planarization [Sheats and Smith 1998].

The planarization can be approximated with a fluid dynamics approach [Sheats and Smith 1998]

$$Planarization \propto \frac{t \gamma \eta h_0^3}{\eta w^4}$$

where t is the leveling time, γ is the surface tension, h_0 is the initial film thickness, η is the solution viscosity, and w is the feature width. This expression shows that planarization is most affected by the feature width and the film thickness. The strong dependence on feature width explains why spin-coating may be good for planarizing local geometries, but is not a good technique for global geometries (>100 microns). The strong sensitivity to film thickness suggests that the planarization layer should be as thick as allowed for improved planarization. This also suggests considering the film thickness when comparing spin-coating results.

Planarization can be best achieved by using materials with a low molecular weight and high solids content [Sheats and Smith 1998] and [Thompson, Bowden, and Willson 1994]. The planarization of 25 micron pitch and 0.8 micron tall features with 2 micron thick PMMA films increased from 30% to over 70% with polymers of molecular weight 500,000 and 30,000, respectively.

Using the fluid dynamics approach approximation from above, the planarization of a film with the same the condition but half as thick (1 micron) would decrease the planarization by a factor of eight.

Another way to improve the planarization is to spin multiple coatings. Multiple coatings of the same material will have no affect on the etching properties. [Thompson, Bowden, and Willson 1994]. Four 0.5 micron coatings rather than two 1 micron of PMMA with a MW of 500,000 increased the planarization by over 20%.

The thickness of spun film is dependant on many parameters – spin speed, solid concentration, and solid molecular weight can be modeled easily. Just as the film thickness increases for lower spin speeds, the film thickness increases for increased molecular weights, and increased solid concentrations. These relationships can be combined [Thompson, Bowden, and Willson 1994]

$$t \propto \frac{A \eta C^2 \omega^{-2}}{\eta^2}$$

where C is the solids concentration, η is the intrinsic viscosity, ω is the spin speed, and A, η , η , and η are constants. Thickness is easily controlled by spin speed, but the spin speed should be not too slow or too fast. Spinning too slow causes lack of uniformity – solvent loss causes dynamic resist viscosity. Spinning too fast causes lack of uniformity from vibration and turbulent air flow over the wafer. High solids concentration can cause radial striations in the film, caused by evaporation driven surface tension effects [Birnie 2000].

2.4.2 Spin-Coating with Reflow

Baking a spun-on film above the film's glass transition temperature can dramatically improve the planarization achieved. In this case, the high viscosity of the film balances the driving forces for flow – capillary and gravity. Capillary forces can be on the order of 1000 times more significant than gravity. The timescale for leveling T is given as

$$T \approx \frac{3\eta w^4}{\gamma^4 h_0^3}$$

where η is the viscosity, w is the feature width, h_0 is the film thickness, and γ is the surface tension [Bornside et al. 1991]. This relationship emphasizes the strong dependency on film thickness and feature width, and suggests good planarization can be achieved if you wait long enough.

Several organic materials have been evaluated as planarizing layers with reflow processing [Stillwagon and Taylor 1989]. The best materials to be used were those capable of long, low viscosity leveling periods. They spun low molecular weight polymer resins and low viscosity liquid monomers into films approximately 2 microns thick over various sized topology that was 1 micron deep. They found heating novolak resin above its cross-linking temperature for two minutes (after which they became solid) achieved better planarization than heating it below its cross-linking temperature for 30 min. Ortho-cresol novolak planarized better than mixed-isomer novolak, which planarized better than novolak-based photoresist. Poly(α -methylstyrene), which does not cross-link at 225°C, planarized best, with 75% planarization of 100 micron features, when baked at 225°C for 10 min. When film were spun thicker, then planarization

improved significantly for both ortho-cresol novolak and poly(? -methylstyrene) – 90% planarization of 100 micron features.

2.4.3 Spin-Coating with Etch-back

Spin-coating a thick film achieves better planarization. After the spin-coating process, the film can be isotropically oxygen etched to reduce its thickness. After it is thinned to a minimal thickness above the high points of the topology, another layer can be spun on top of it. This can be repeated, or done only once.

Etching processes can expose the wafer surface to contaminants, but with a clean etcher and carbon wafer chuck this may be avoided. These contaminants would cause micro-masking of the planarization layer, increasing the roughness and locally decreasing the planarization.

2.4.4 Chemical-Mechanical Polishing

Chemical-mechanical polishing (CMP) is a planarization method that uses a slurry of chemicals and abrasive particles and a polishing pad. By moving the wafer in circular, linear, or elliptical motions across a much larger spinning pad, the surface of the wafer is planarized. The CMP process is used for the planarization needed to isolate and connect transistors on a chip [Sing and Bajaj 2002]. Both metals and oxides can be planarized by this process to the nanometer scale. A thorough description of the CMP process, as well as state of the art advances in CMP technology has been given [Singh and Bajaj 2002].

CMP cannot be used for the planarization needed for this thesis [Onsongo 2002]. The slurry particles not removed after the process can cause serious defects in the devices on the wafer. The CMP process is relatively dirty and cannot be used for this step in the fabrication process because of the sensitivity to contaminants. Although CMP is used in full scale manufacturing, it will not be considered for this thesis.

2.4.5 Contact Planarization

Wafer surfaces can be planarized by using processes that come into direct contact with the wafer with an optically flat substrate. Techniques used for imprint lithography can also be used for contact planarization. The processes need to be modified so that the master or template has no features or pattern to be transferred. This should not be a problem because the master or template is flat before it is patterned to be used to imprint with. The processing to make the template should be the same except the patterning and pattern transfer used to create the templates. Thermal imprinting and S-FIL imprinting are techniques that can be used.

2.4.5.1 Thermal Imprinting

Thermal imprinting is done by pressing a mold onto a film that is heated above its glass transition temperature. The film and mold are pressed together for some time to allow the film to flow to fit the mold. After this time they are cooled, and then separated. This technique has been demonstrated by many

[Chou 2001], [Schultz et al 2000], [Sheer et al. 1998], [Jaszewski et al. 1998]. Chou has described planarizing 200nm deep steps by heating both PMMA and novolak resin at 175°C, and applying 600 psi.

2.4.5.2 S-FIL Imprinting

S-FIL imprinting can be used to planarize topography. This can be done by using The S-FIL process, a featureless S-FIL template, and a purely-organic UV curing monomer solution. The S-FIL process has been demonstrated over patterned topography [Colburn, Grot, and Choi et al. 2001]. A organic solution was UV-cured to make a planarization layer over 700nm tall, submicron wide features.

The S-FIL planarization method does not create 100 % planarization because of densification during curing. Polymerization is often accompanied by a volumetric shrinkage. The densification of polymers between constrained surfaces with topology has been studied [Colburn 2001]. The comparison between the shrinkage of an unconstrained thin film and a film constrained by its bottom and edges was modeled with finite-elemental analysis (FEA). A film that shrinks 27 % volumetrically shrinks 10 % in every direction when unconstrained. The film constrained on its edges and its bottom shrinks approximately 20 % vertically (where the vertical direction is orthogonal to the plane of the film).

The shrinkage of a thin film constrained between a relatively rigid template with 100 nm wide, 200 nm tall lines and a thicker film was also modeled with FEA. The curing film was modeled to shrink volumetrically by 27 %. The

surface of the shrinking film next to the featured template shrank predominately in the vertical direction (orthogonal to the plane of the film). In the areas without the lines, the film shrank uniformly vertically, by about 20 %.

This analysis can be used to approximate the shrinkage of a film between topography and a planarizing (blank) S-FIL template. The towers on the film in the FEA simulation are analogous to trenches in a substrate, although the features of the ACTIVE pattern in the substrate are one to two orders of magnitude larger in the lateral dimension than the towers modeled. The 3 to 23 micron lateral dimensions of the ACTIVE patterns compared to the quarter-micron topology height, may allow a good approximation of the shrinkage at the center of the features to be equal to the shrinkage of a featureless film that has the thickness of the nominal film thickness plus the topology feature height.

With this assumption, the planarization degradation is proportional to the topology height. If the monomer nominal film thickness h shrinks by vertically by 20 % when cured, the vertical distance shrunk is h times 20 %. Inside the active area, the monomer film thickness is $h + d$. After curing the vertical distance shrunk is $(h + d)$ times 20 %. The difference in the vertical distance shrunk between the two regions produces a depression in the surface of the once-flat film. Using the large lateral distance approximation, the depth of this depression is independent of the film thickness h and is equal to d times 20 %. Assuming the UV-curing planarizing film shrinks 27 % volumetrically and 20 % vertically when constrained and the topology height is 250 nm, the depression depth from curing would be 50 nm. This vertical shrinkage can be related directly

to percent planarization (assuming the imprint is flat before the curing). If the depression depth is 0.2 times d , then the planarization is 80 %.

A solution of 96 wt% cyclohexyl acrylate (CHA), 1 wt% SIB1402 (cross-linking agent), and 3 wt% Irgacure 184 and Irgacure 819 mixture (free radical generators) will volumetrically shrink 8.6 % [Colburn 2001]. Colburn also showed that the displacement of a constrained film decreased linearly with decreasing linear coefficient of expansion. With a linear assumption, the CHA should vertically shrink less than 8.6 % (about 7 %) and cause a depression in the surface of a planarizing imprint above a 250 nm deep feature that is about 20 nm deep, or 93 % planarization.

2.5 PLANARIZATION EXPERIMENTS

Planarization methods were tested in order to find a preferred approach for the planarization needed. Spin-coating was the first planarization method tested. Materials that have been used as transfer layers for the S-FIL process were used first because of their availability. The next method tested was reflow, using a novolak resin and a novolak based photoresist. Finally the S-FIL planarization method was tested using CHA and a mixture of CHA and a crosslinking agent.

2.5.1 Spin-Coating Experiments

Spin-coating was the first method tested for its planarization properties. The first materials tested were a negative photoresist, HR 100, produced by Olin-Hunt, and a backside anti-reflective coating (BARC), Barli (all Barli used in this

thesis was 0.25 micron), produced by Clariant. They both have been used as a transfer layer for S-FIL processing, but had not been tested for planarization. The Barli was designed to be spun to 0.25 microns thick, and to conform to topography (to act as a BARC). The two products were spun onto dummy Si wafers with an oxide film deposited that was wet-etched with the ACTIVE pattern, to test the planarization of topography.

HR 100 was spun with varying conditions of maximum spin speed, acceleration, the number of coats spun, and % solids. The pre-spinning preparation, solution dispense, total time of spinning, spinning environment, baking time and temperature, and UV exposure conditions were held constant.

For the HR 100, the maximum wafer speeds used were 2700 rpm and 3750 rpm. The acceleration was varied to 100 rpm/s, 300 rpm/s, and the maximum acceleration of the machine, which got the wafer to the maximum speed in approximately one second (approximately 4000 rpm/s). Wafers were spun with one, two, and three coats. The composition of the HR 100 was uncertain, but the % solids were varied by spinning the original formulation, and also a mixture of 1:1 HR100: xylenes (its solvent), which reduced its % solids by half.

The wafers were cleaned before the spinning with a 2:1 Sulfuric Acid: Hydrogen Peroxide (Piranha) clean, followed by a copious DI water rinse, and dried in a spin-rinse-dryer (SRD). For each wafer one cc of the liquid was hand dispensed with a polypropylene micropipette onto a static wafer, and allowed to sit for 2 seconds before beginning to spin. Each wafer was spun for a total of 60

seconds, and then promptly placed on a hot plate set at 138°C. The wafers were allowed to bake for 1 min, and then cool on a cleanroom wipe on a tabletop. The HR 100 was exposed with a UV lamp for 1 min, and then put on a hot plate set at 170°C. The wafers were allowed to bake for 90 sec, and then cool on a cleanroom wipe on a tabletop.

The Barli was spun onto a wafer with one coat, and another wafer with two coats (the first coat was baked before spinning the second). The pre-spinning preparation, solution dispense, total time of spinning, spinning environment were the same as used with the HR 100. The wafers were both spun with maximum acceleration of the machine, the maximum spin speed of 4000 rpm, bake temperature of 180°C, and baking time of 1 min., and the solution was not altered. Barli is made of 90% cyclohexanone and of 10% trade-secret resin (unspecified MW).

The planarization achieved and the spun film thicknesses were measured on a Tencor Alpha-step profilometer. The planarization of 10 micron and 150 micron wide trenches near the center of each wafer was measured. The trench widths measured were chosen for ease of measurement and to evaluate the planarization of a full range of topology. The 10 micron lines will be planarized better than the largest active areas needed to be planarized, and the 150 micron lines indicate the planarization of the largest features on the templates (not associated with MOSFETs). The thickness measurement was made by scratching away a thin strip of the film with a razor blade, and profiling the scratch. The planarization was calculated by measuring the trench depths of the etched oxide

surface before planarization, and by measuring the depth of the depression in the surface of the planarization film.

The results of the spin-coating of HR 100 and Barli are shown in Table 2.1. The data are arranged in columns, with each row representing the results from a different trial. The type and/or dilution column describes the material used, where HR 100 1:1 represents the 1:1 diluted solution of HR 100 with xylenes. The original trench depth represents the uncoated feature height; the spun film thickness represents the film thickness measured on top of the oxide layer that was etched. The planarization was calculated using the measured values of the depth of the depressions and the percent planarization formula defined in the beginning of second section of this chapter. The dummy wafers used for these trials had topography of 180 nm and 210 nm. The lower topography, although not representative of the 250 nm topography needed to be planarized, did prove useful, because the planarization trials failed to planarize the topography well. From this one can deduce that taller topography will be planarized to a lesser degree. The undiluted HR100 spun a film thicker than a micron, and did not planarize even the 10 micron trenches to the requirement (increased planarization is needed for a thicker film). The diluted HR 100 was used for the remainder of the HR 100 spinning. The remaining trials showed some variation in planarization, with the best planarization achieved by the triple coated wafer. This was done over 180nm deep trenches - linearly interpolating for 250nm trenches predicts a planarization of 46 %. Barli did not planarize well, with a maximum planarization of 24 % with a 570 nm thick film over 210 nm

topography. Assuming the same 10 % trend of planarization improvement per coat, the planarization achieved by two more coats would not be sufficient. In summary, the HR100 and Barli did not planarize the topography well enough to be used for the MOSFET process.

Type and/or Dilution	Max RPM	Acceleration, rpm/s	Coats	Original Trench Depth, nm	Spun Film Thickness, nm	150 Micron Trench Planarization, %	10 Micron Trench Planarization, %
HR100	3750	Max	1	180	1200	22	56
HR100 1:1	3750	Max	1	180	320	22	44
HR100 1:1	2700	Max	1	180	400	22	47
HR100 1:1	3750	300	1	180	525	28	42
HR100 1:1	2700	300	1	180	475	22	47
HR100 1:1	2700	100	1	180	610	33	56
HR100 1:1	3750	Max	2	180	640	28	53
HR100 1:1	3750	Max	3	180	900	22	64
Barli	4000	Max	1	210	280	14	14
Barli	4000	Max	2	210	570	14	24

Table 2.1. Planarization results from spin-coating HR100 and Barli.

2.5.2 Spin-Coating and Reflow

The second method for planarization tested was spin-coating and reflow. A (mixed isomer) novolak resin in propylene glycol monomethyl ether acetate (PGMEA) and a positive photoresist (AZ 5209) were spun over dummy wafers with the ACTIVE topography. After spinning, the films were baked above their cross-linking temperatures (170 °C) and allowed to reflow.

The novolak resin was mixed with PGMEA to form a solution with 15 % solids. Solutions of 30 % and 20 % were spun, but the films spun were of poor quality, with a uniform distribution of radial striations of non-uniform film thickness. This surface relief is thought to arise because of evaporation driven

surface tension effects [Birnie 2000]. The novolak solution and the positive photoresist were spun with the same conditions, except three coats of the novolak were needed to achieve a one micron film, and only one coat of the photoresist was needed. The novolak is a thermosetting polymer and was crosslinked by heat after each film was spun, so that the 2nd and 3rd films would not dissolve the films previously spun.

After one minute at 100°C, the wafer was placed on another hot plate that was 205°C and allowed to bake for 10 min. After which the wafers were allowed to cool on a cleanroom wipe on a tabletop. After the novolak wafer was cooled, the second and third coats were applied in the same fashion.

The planarization achieved and the spun film thicknesses were measured on a Tencor Alpha-step profilometer. The planarization of 25 micron wide trenches near the center of each wafer was measured, and 10 micron trench on the novolak wafer. The thickness measurement was made by scratching away a thin strip of the film with a razor blade, and profiling the scratch. The planarization was calculated by measuring the trench depths of the etched oxide surface before planarization, and by measuring the depth of the depression in the surface of the planarization film.

The results of the spin-coating of novolak and positive photoresist are shown in Table 2.2. The data are arranged in columns, with each row representing the results from the two wafers. The spun film type column describes the material spun, and the bake temperature and time describe the second baking step where the materials would reflow. The positive photoresist

was spun onto a dummy wafer with a single film of cross-linked Barli already spun onto it. This Barli film accounts for about 280 nm of the final film thickness, and partially planarized the topography. Since the wafer with the photoresist and Barli did not planarize well, the novolak film was still over a micron thick, and the Barli film would improve the planarization, this trial was not repeated with photoresist spun onto a Barli-free wafer. The number of coats used described the number of coats where reflow was used. Although the wafer with the positive photoresist had two films – the Barli and the photoresist, only the photoresist was suspected to reflow. The original trench depth represents the uncoated feature height; the spun film thickness represents the film thickness measured on top of the oxide layer that was etched. The planarization was calculated using the measured values of the depth of the depressions and the percent planarization formula defined in the beginning of second section of this chapter. The dummy wafers used for these trials had topology of 230 nm and 245 nm. The lower topography, although not representative of the 250 nm topography needed to be planarized, did prove useful, because the planarization trials failed to planarize the topography well. Neither of the films planarized the 25 micron wide trenches to the degree needed for the MOSFET process. The planarization done by the novolak of the 10 micron wide trenches that were 230 nm deep suggests that this planarization method could be used to if only sub-10 micron features needed to be planarized. But this would not be suggested, because the planarization achieved is only marginally greater than the specification.

Spun Film Type	Reflow Bake Temp., °C	Bake Time, minutes	Coats	Original Trench Depth, nm	Spun Film Thickness, nm	25 Micron Trench Planar., %	10 Micron Trench Planar., %
Novolak, 15% solids	205	10	3	240	1000	22	67
Positive Photoresist AZ 5209 on Barli	205	10	1	245	1375	33	-

Table 2.2. Planarization results from spin-coating novolak and positive photoresist and allowing to reflow.

2.5.3 Spin-Coating and Imprinting

2.5.3.1 Introduction

A combination of spin coating and S-FIL imprinting was used to planarize dummy wafers with the ACTIVE topography, similar to those used in the spin-coating experiments. The imprinting was done on top of a spun layer of Barli (0.25 micron), and Barli (0.25 micron) was spun on top of the imprint. The lower Barli film was used for its proven ability to provide a good surface to imprint upon. The upper layer of Barli was used to ensure that the monomer used in the patterning imprint does not mix with the planarization layers. This was done because the acrylate monomers in the etch barrier are similar to the acrylates used in the planarization imprint, and the “like dissolves like” principle. The exposure of the monomer solution to the cure imprint would cause swelling and associated problems.

The wafers were cleaned before the spinning with a 2:1 Sulfuric Acid: Hydrogen Peroxide (Piranha) clean, followed by a copious DI water rinse, and dried in a SRD. One cc of the Barli (0.25 micron) was hand dispensed with a polypropylene micropipette onto a static wafer, and allowed to sit for 2 seconds before beginning to spin. Each wafer was accelerated to 4000 rpm in about a second and spun for a total of 60 seconds, and then promptly placed on a hot plate to bake (to drive out the solvents, anneal the film, and cross-link the Barli). The first Barli film was baked on a hot plate that was 180°C, and the second Barli film was baked on a hot plate that was 160°C (to minimize shrinkage of the CHA imprint).

The planarizing imprint was made with the S-FIL overlay alignment machine using a featureless S-FIL template, and a monomer solution based on the cyclohexyl acrylate (CHA) monomer. The first solution used was 96 wt% CHA and 4 wt% Darocur 1173 (photo-initiator). It was shown to shrink during the baking of the 2nd Barli coat or to mix with the Barli solution spun on top of it. A new solution was made, with a cross-linking agent added. The cured planarization imprint would be significantly less miscible with the cyclohexanone if it were highly cross-linked. The new cross-linking CHA solution (XCHA) was 48 wt% CHA, 48 wt% ethylene glycol diacrylate (EGDA) (cross-linking agent), and 4 wt% Darocur 1173. The planarization achieved by this new mixture was shown to not degrade with the second Barli layer.

In order to minimize the thickness of the planarizing imprint, the imprint was made by “partial filling”. Partial filling means that not enough monomer

solution was dispensed to completely fill the template area during the imprint. This causes the imprint to be round and smaller than the size of the template. The thickness of the imprint is generally thinner than if more liquid were dispensed. The imprint is only in the center of the imprint and not at the edges. This asymmetric loading causes the template to bow slightly, causing the imprint to have a gradual dome shape with a maximum thickness in the center. Before the imprinting, the featureless S-FIL template had a surface flatness of approximately 20nm across the 1” template. The bowing from the asymmetric loading, as well as asymmetric holding of the template and dispensing of the monomer drop caused some variation in the imprint’s thickness.

2.5.3.2 Planarization and Thickness Measurement

The variation in thickness gave reason to measure the thickness and planarization in an array of places across the imprint, to better characterize this planarization method. The measurements of the thickness and planarization of the planarization layers were done with a Tencor Alpha-step profilometer, after the 2nd Barli layer was spun. The measurements were taken one side of three die that the imprint was on top of. Figure 2.6 shows the locations of the measurements across each die. The 30 arrows on the die indicate the places of the measurements, and the numbers designate the trends of the numbering of the measurements. One die is shown for clarity, but measurements were taken at 30 places on each of the die (90 places total). The pattern shown is the POLY pattern, and but it serves to show the distribution of the measurements across the

die. The flatness of the surface was measured to calculate the planarization at every location on the wafer, and then the wafer was scratched with a razor blade in rows along each die so that the thickness of the films in each place could be measured. The thicknesses measured are the sum of the planarizing imprint and the Barli films. Most of the flatness measurements were made across 10 micron wide features, for the ease of measurement. Measurements 1 through 6 were made across 150 micron trenches, and the measurements made shown on the left side of Figure 2.6 (30, 29, 24, 23, 18, 17, 12, and 11) were made across features 10-30 microns wide.

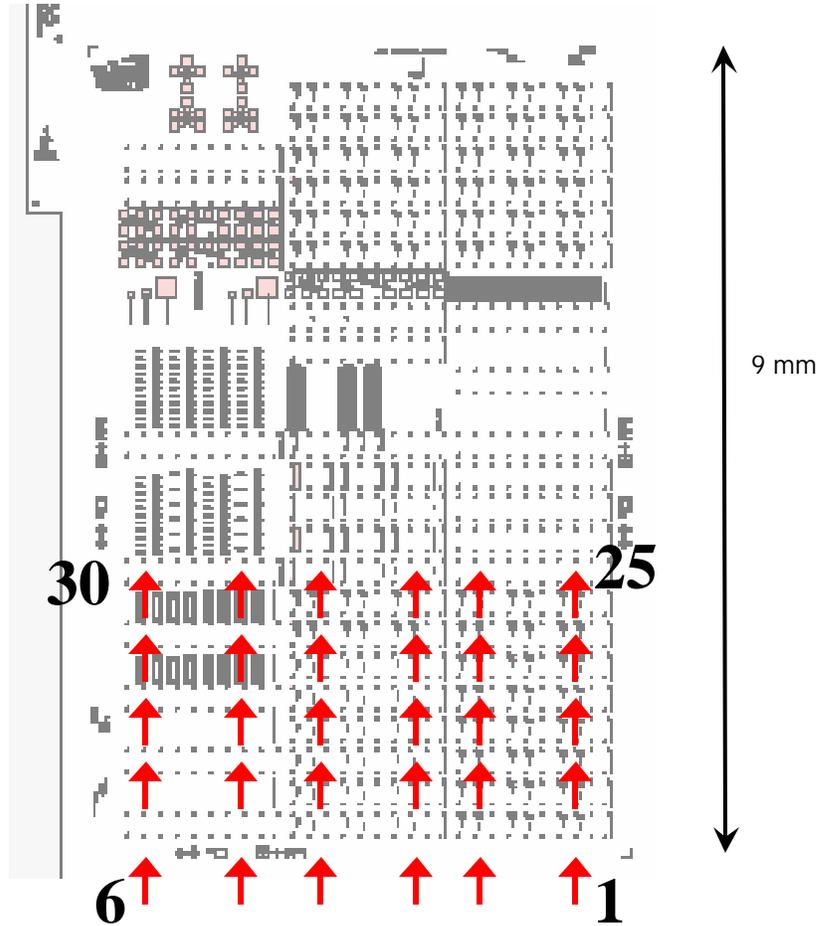


Figure 2.6. A single die showing where the thickness and planarization measurements were taken.

2.5.3.3 Results and Discussion

The Barli/CHA/Barli combination planarized the ACTIVE topology quite well, but the topography of the top surface of the planarization layers was troubling. Ridges formed on the sides of the planarized trenches. These ridges

were not seen in the previous spin-coating experiments, and warranted further investigation. A wafer was planarized in a similar manor - Barli, then the CHA imprint, and finally another Barli coat, but the flatness of a trench was measured after each step. Images showing the progression of the planarization are shown in Figure 2.7. The images are photographs of the profilometer monitor showing the surface scans. All of the images show the planarization of 10 micron wide, 210 nm deep trenches on a dummy wafer. The leftmost image shows the surface flatness after the first Barli coat – a 180 nm deep depression (14 % planarized). The center image shows the surface after the CHA imprint – a 25 nm deep depression (88 % planarized). The rightmost image shows the flatness after the second Barli coat. The surface has a 50-60 nm deep depression, but also 30-45 nm tall ridges on either side of the depression. Not only is the second Barli coat forming ridges on either side of the depression, the Barli is degrading the planarization of the depression.

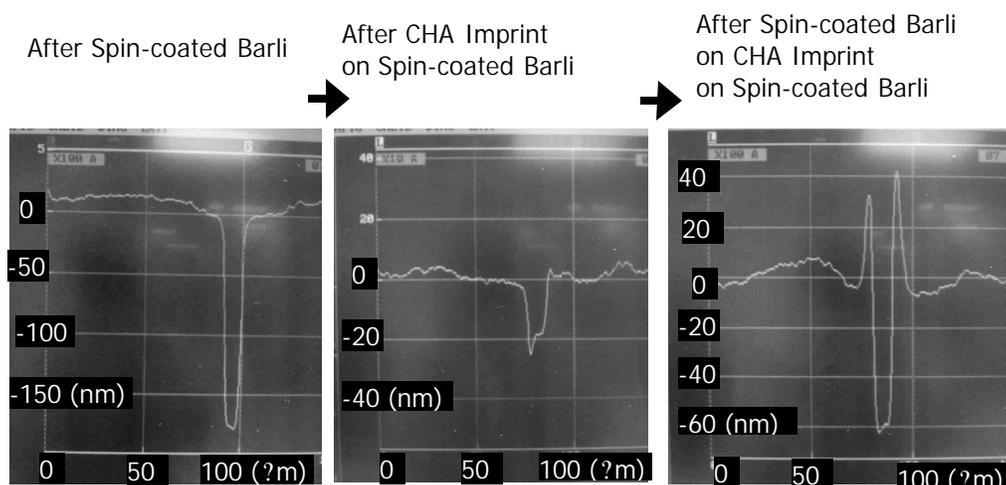


Figure 2.7. Profilometer scans showing the progression of planarization with Barli, CHA Imprint, and then Barli.

Either the CHA imprint was dramatically shrinking during the baking of the 2nd Barli coat, or the cyclohexanone in the Barli solution was mixing with the cured CHA imprint. In order to make the CHA imprint more resistant to the baking or the solvent, a new solution was made, with a cross-linking agent added. The cured planarization imprint should be significantly less miscible in the cyclohexanone if it were highly cross-linked. The new cross-linking CHA solution (XCHA) was 48 wt% CHA, 48 wt% ethylene glycol diacrylate (EGDA) (cross-linking agent), and 4 wt% Darocur 1173.

The solution was used, and the flatness of 10 micron trenches was measured after each major step in the planarization process. Images showing the progression of the planarization are shown in Figure 2.8. All of the images show the planarization of 10 micron wide, 220 nm deep trenches on a dummy wafer. The leftmost image shows the flatness after the first Barli coat – a 180 nm deep depression (18 % planarized). The center image shows the surface after the CHA imprint – a 20-30 nm deep depression (91-86 % planarized). The rightmost image shows the flatness after the second Barli coat. The surface has a total flatness of 20 nm, and the depression from the trench is not discernable in the variation in the surface. The shrinkage of the XCHA imprint during curing can be approximated from the left and center images. The XCHA imprint shrank to make a 20-30 nm depression over the 180 nm depression in the surface of the Barli. This fraction gives the percent shrinkage – 11-17 %. Although a CHA solution mentioned in section 2.X should shrink less than 9 %, adding the cross-linker should increase the shrinkage. The shrinkage of a solution of SIA 0210 (silylated monomer) and

cross-linker increased approximately 2 % for the first 5 % cross-linker added [Colburn 2001]. Fortunately, the planarization did not degrade with the baking of the 2nd Barli coat.

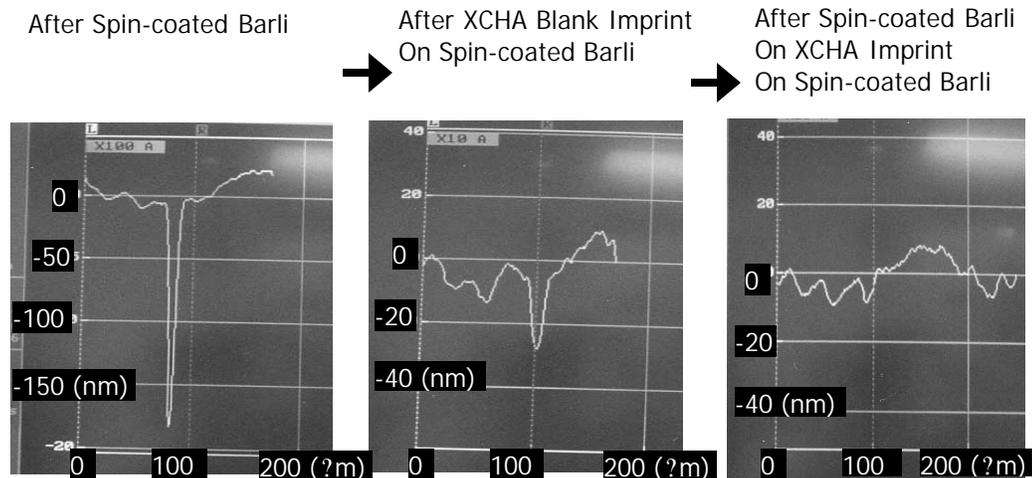


Figure 2.8. Profilometer scans showing the progression of planarization with Barli, XCHA Imprint, and then Barli.

An image from a photograph of a wafer with part of the ACTIVE pattern planarized by Barli, XCHA, and Barli are shown in Figure 2.9. This wafer has the ACTIVE pattern etched into a 240 nm thick layer of oxide. On top of the image is a dashed line in the shape of square, representing the area of the wafer that is imprinted upon. Three dies of the ACTIVE pattern are in the right side of the square, and the left half of the square has no dies. The center of the square is a planarizing imprint. The dies in the square are numbered 1-3, for clarification in the thickness and flatness measurements.

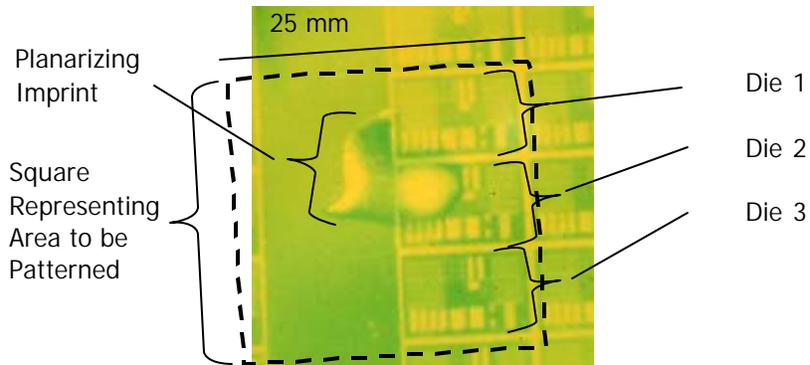


Figure 2.9. Image of a photograph showing a planarizing imprint on the ACTIVE pattern, also designating the numbering of dies 1-3.

Figure 2.10 includes a plot showing the thickness variation of the planarization layers across dies 1-3 defined in Figure 2.10. The measurements were taken as shown in Figure 2.6. The depth of the topography planarized was 240 nm. The range of thicknesses measured was 535 nm to 635 nm. The thicknesses are greatest in the center of the plot, showing the location of the imprint. The placement of the imprint on this plot can be compared to the photograph in Figure 2.9; the imprint is partially in die 1, and not in die 3. The thickness is uniform on the left and right sides of the plot, indicating the areas of the wafer where the imprint did not reach.

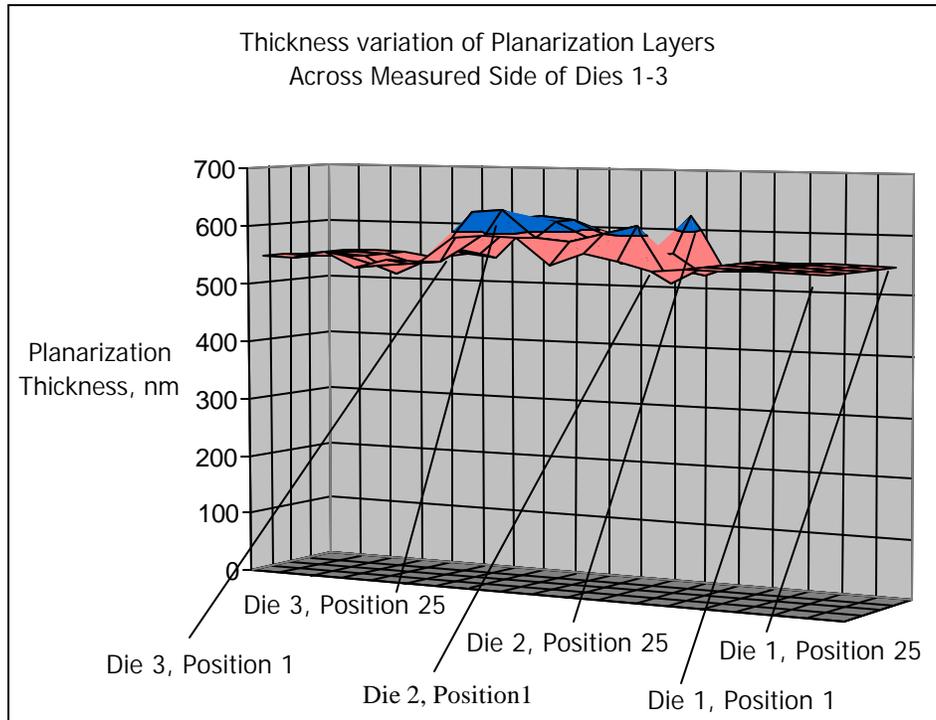


Figure 2.10. Thickness variation of planarized layers across the measured side of dies 1-3.

Figure 2.11 includes a plot showing the planarization variation of the planarization layers across the dies 1-3 defined in Figure 2.10. The wafer is the same as shown in the previous two figures, and has topography 240nm deep. The measurements were taken as shown in Figure 2.6. The values plotted are the depression depths measured at the various locations. The values range from 230 nm to 10 nm. It is obvious where the XCHA reached – the center of the plot shows dramatically lower values than the sides. The 10 μ m wide trenches were planarized to 10-30 nm (96-88%), and 150 μ m wide trenches were planarized to 20-40 nm (92-83%). This variation is most likely due to the partial planarization

of the first Barli layers. The Barli will planarize the 10-micron trenches significantly more than the 150-micron trenches. The increased topography height of the wider trenches causes a deeper depression in the XCHA imprint from the shrinkage.

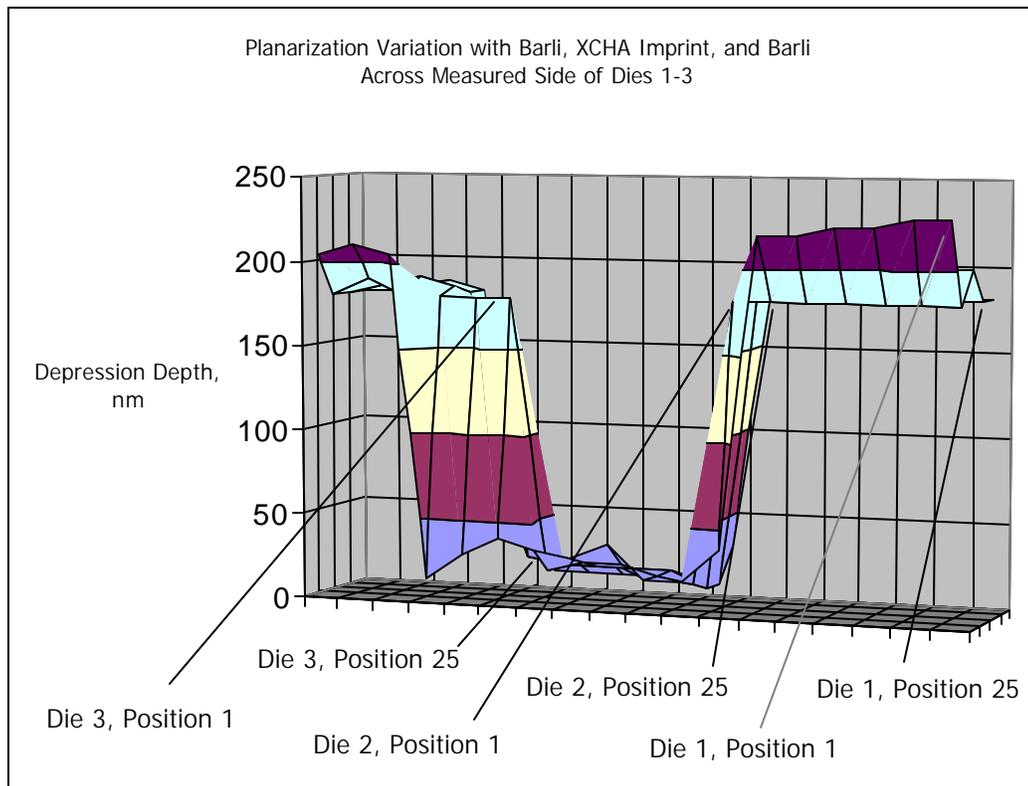


Figure 2.11. Planarization variation with Barli, XCHA Imprint, and Barli across the measured side of dies 1-3.

The Barli-XCHA-Barli planarization process achieves the planarization needed for the S-FIL process to be used in the fabrication process of MOSFETs. It was used to planarize the topography on wafers used for the alignment and imprinting demonstrated in Chapter 3.

2.5.3.4 Measuring Thickness

It is not obvious how the thickness of the planarizing imprint is measured. One method may be by using ellipsometry. This would be difficult to measure accurately because of the multiple films. After the planarization, there are the 2 Barli films, the XCHA imprint, the oxide hard-mask, and the POLY (assuming the thickness is measured in a place where the isolation oxide has been etched). Rather than use ellipsometry, the thickness can be measured after the POLY patterned imprint - by dicing the wafer so that the edge runs through the planarizing imprint near were the MOSFETs to be made are. The half with the MOSFETs is processed (at a premium), and the other half is inspected with the SEM. By viewing the cross-section of the wafer, the thickness of both the etch barrier imprint and the planarization layers can be measured. Figure 2.12 shows a cross-section of such a wafer. The layers can be seen clearly.

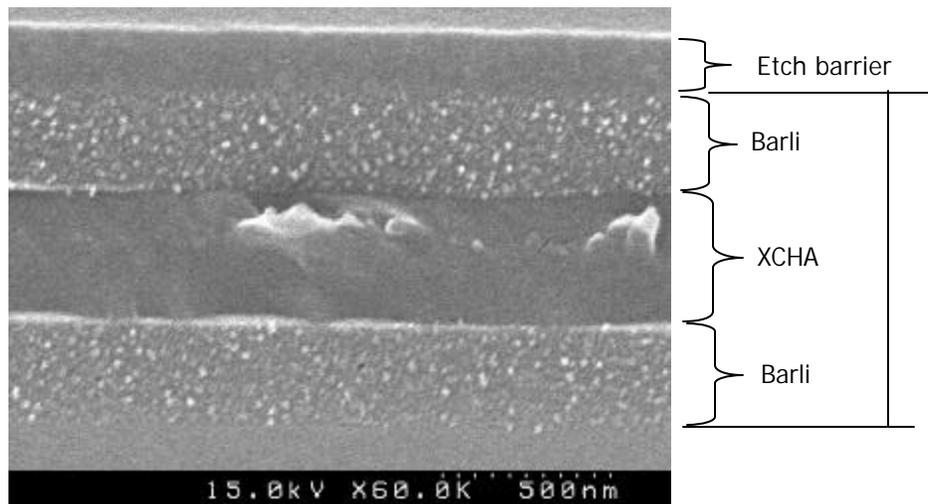


Figure 2.12. Cross-sectional view showing the thickness of the planarization layers.

2.5.3.5 Etch Transfer

The planarizing imprint must be able to transfer the imprinted pattern from the etch barrier. Figure 2.13 shows an SEM image the transfer of a dot pattern through layers of Barli, XCHA, and Barli. The circular pattern transferred through the planarization layers makes a tower with clearly defined strata. The etch barrier is the top layer, with layers of Barli, XCHA, and Barli below. The area around the tower is covered in smaller features that are not supposed to be there. They are the result of a micro-masking problem discussed in Chapter 4. The pattern is transferred through the three layers, with no abrupt changes at the XCHA-Barli interfaces.

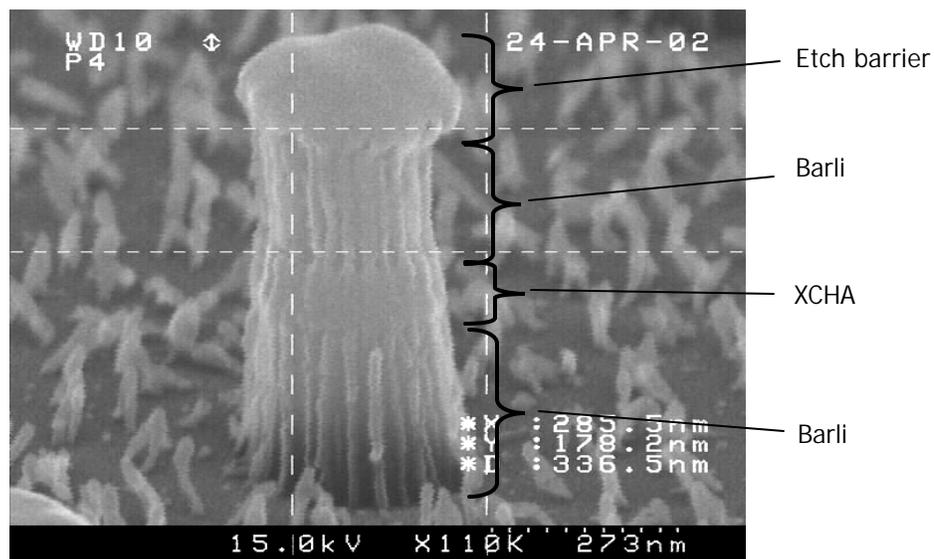


Figure 2.13. Transfer of a dot structure through the planarization layers.

Chapter 3: Imprinting and Alignment

3.1 INTRODUCTION

The goals of the imprinting and alignment process are defined discussed. Afterwards, the tool which will be used for this process development, the S-FIL overlay alignment machine, is discussed. Next the imprinting and alignment with the tool is explained along with the parameters that will adversely affect the process. Then the methods of evaluating the process are described, followed by the imprinting and alignment results.

3.2 GOALS OF IMPRINTING AND ALIGNMENT

The goal of this chapter is to explain the imprinting and alignment needed for the thesis and evaluate the process. The goals of the imprinting and alignment process are to align the POLY pattern over the ACTIVE pattern, and cure an imprint with a thin uniform residual layer, to transfer as many gate structures as possible.

The alignment has a defined specification of +/- 2 microns in X and Y (see Figure 3.1). The θ alignment is a parameter that is adjusted, but not significant for this project. If the patterns are misaligned in θ so that the difference in X and Y alignment is 4 microns across 20 mm, the θ is misaligned by approximately 1/100 of a degree.

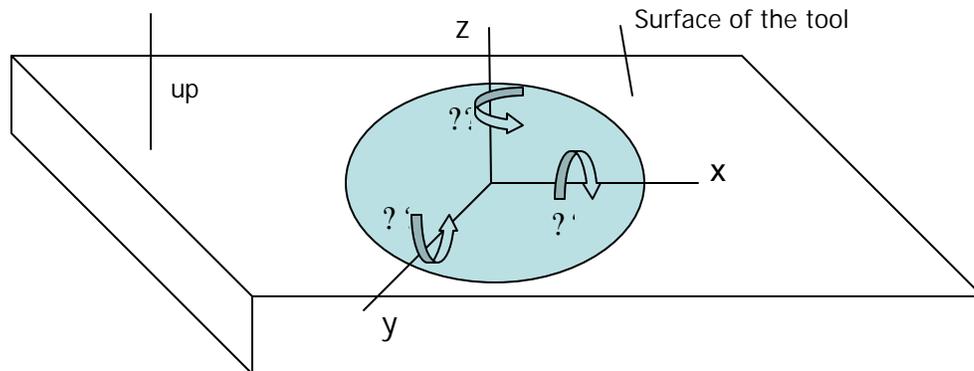


Figure 3.1. Definitions of directions of coordinates used in this chapter.

The allowable variation in the pattern can be approximated by 10 % of the minimum feature size used. In this case the minimum feature sizes are the gate lengths, which vary from microns to less than 0.1 micron. The maximum nominal thickness of the residual layer of the imprint is still relatively arbitrary chosen to be 250 nm.

As mentioned in the previous chapter, the area of the pattern transferred is dependant on the planarization flatness. The allowable flatness variation is dependant on the variation in thickness of the etch barrier residual layer. The spin-coating and imprinting planarization process produces the flattest surface or the methods tested, but the planarization imprint varied in nominal thickness. This variation can be considered variation in flatness. If the allowable flatness of the planarization layer is 110 nm minus the variation in etch barrier residual layer thickness, and the spin-coating and imprinting planarization method planarizes the topography to 30 nm, the combined deviation in planarization layer thickness and etch barrier residual layer thickness is 80 nm. This relationship imposes a

maximum variation in etch barrier residual layer thickness of 80 nm, but the practical limit is actually less. This small variation suggests that only a small area of the patterned imprint is going to be transferred. This is acceptable for the process development of a proof-of-concept project.

3.3 S-FIL OVERLAY ALIGNMENT MACHINE (OAM)

The OAM was developed to demonstrate layer-to-layer alignment with S-FIL [Choi et al. 2001]. The OAM is a Canon 501 parallel light mask aligner that has been modified to implement a multilayer S-FIL process. The original mask holder was modified to hold a low-profile 2-degree-of-freedom tip/tilt flexure with a mating S-FIL template holder (see Figure 3.2 and Figure 3.3). The bulk of the machine is below the level of the template holder; above the template holder is a microscope and exposure assembly. This assembly is used for the blanket UV exposure of the S-FIL process, and for looking through the template to align the features of the template to those on the wafer. The image of the features on the template and wafer are focused on a CCD camera, which is displayed on a monitor. The assembly is normally directly above the wafer/template stack, but can pivot to the side for removal of the template holder and the wafer. Figure 3.2 shows two views of the OAM – with the microscope and exposure assembly pivoted to the side (left) and directly over the wafer (right).

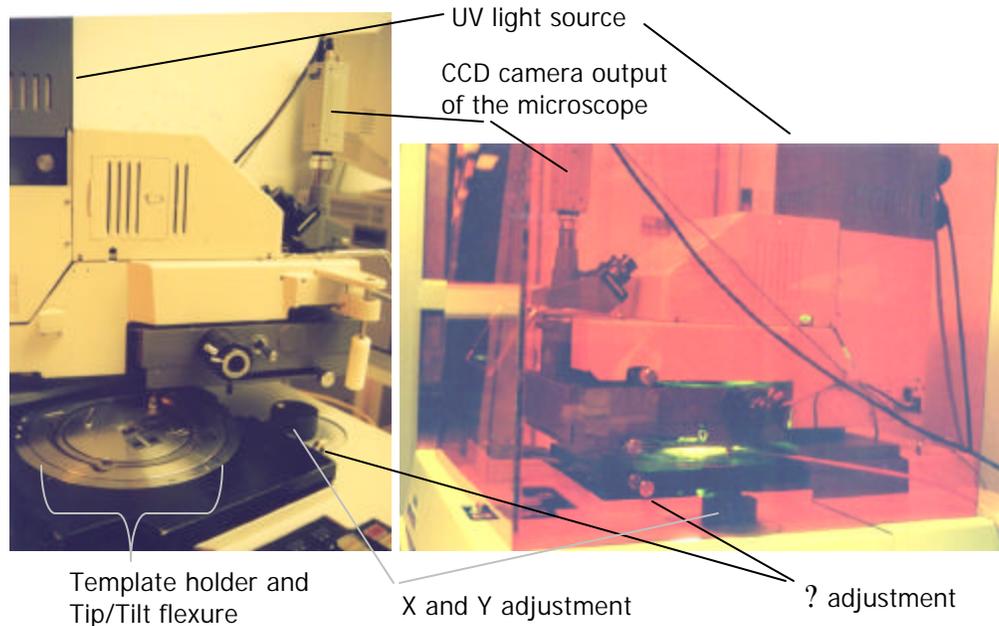


Figure 3.2. Two views of the S-FIL OAM – with the microscope and exposure assembly pivoted to the side (left) and directly over the wafer (right).

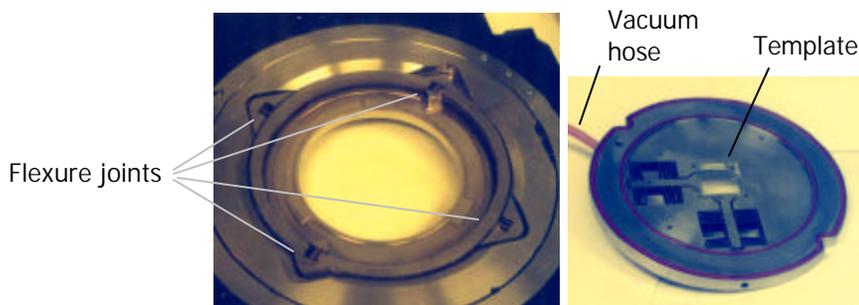


Figure 3.3. The S-FIL tip/tilt flexure assembly (left) and template holder (right).

The lower parts of the machine contain the template and wafer holding and alignment assemblies. The template holder and tip/tilt flexure assembly can be seen on the machine in the left image of Figure 3.2. Figure 3.3 shows the template holder (right) and tip/tilt flexure (left) separate from the machine. The

tip/tilt flexure is mounted to the frame of the machine above (and around) the wafer, wafer-chuck, and XY adjustment assemblies. The template holder assembly sits on the tip/tilt flexure and is held in place by a vacuum pulled in the outer margin of the template holder. The template is held in the template holder by set-screw-driven pistons. The wafer chuck is below the template holder, and is attached to an air piston by a spherical bearing.

The alignment of the template to the wafer is done with the combination of passive and active elements. Figure 3.1 defines the directions of coordinates for this description. The wafer chuck is pushed upwards toward the template to imprint, narrowing the gap in the z direction by the air pressure in the air piston, and dampened by the etch barrier film between the template and the wafer. Rough alpha and beta alignment is achieved by a pre-calibration step utilizing the spherical bearing below the wafer chuck and the tip/tilt flexure. The wafer chuck is brought up and the top-side of a lower extremity of the chuck comes into contact with the bottom-side of the flexure ring. Fine alpha and beta alignment is achieved passively during imprinting with the tip/tilt flexure. The tip/tilt flexure was designed for selective compliance for passive alignment in the α and β motions, with the center of rotation at the template/wafer interface, with low deflections x, y, and z [Choi et al. 2001]. α is adjusted by rotating the template via the tip/tilt flexure and template holder assembly. The range of motion for theta is about 10 degrees, and continuous with no noticeable backlash. X and Y adjustment is done with the original mask-aligner mechanisms. This adjustment has +/- 0.1" range in X and Y and 0.5 micron resolution, and has no problem

moving the wafer when it is in full fluid contact with the template. Submicron alignment has been demonstrated with this machine [Choi et al. 2001]. The machine is not capable of magnification or distortion corrections.

The machine was not designed to have a high throughput - the OAM is designed to only imprint on the center of 4" wafers. There is the capability for XY movement of the wafer chuck relative to the template assembly, but the range-of-motion is used for layer-to-layer alignment only. There is only one microscope objective, so X,Y, and θ alignment is an iterative process. For each imprint, the exposure and microscope assembly is pivoted to the side, the template holder is removed, a new wafer is placed on the wafer chuck, the monomer solution is dispensed, the template holder is put back in place, and the exposure and microscope assembly pivoted back to center. The placement of the wafer on the wafer chuck is important – the wafer must be placed within motion range of the X,Y, and θ adjustments. The monomer solution is dispensed by hand with a micropipette, a process that allows for error in dispensed volume and drop placement. The volume of monomer dispensed is important, because the residual layer thickness of the imprint is determined by the volume dispensed. A thin layer is desired, and thus a low volume, but enough fluid must be dispensed to ensure fluid contact between the template and the wafer for alignment.

3.4 IMPRINTING AND ALIGNMENT PROCESS

First the template is loaded into the template holder. Then the wafer is loaded on the wafer chuck so that the pattern to be imprinted on the wafer is in the

approximate center of the +/- 0.1" X and Y range of the tool. This is done by lowering the wafer chuck and positioning the objective over a specific area on the template. Then the template holder is removed and the wafer is raised up into the view of the microscope and positioned until the same specific area on the wafer is positioned under the objective. Then the monomer is dispensed, and the template and wafer are brought into contact. After the monomer has spread and filled the area between the template and the wafer, the alignment process begins.

The imprinting and alignment process is long and iterative with the OAM and the S-FIL MOSFET templates. The process is so iterative because the alignment is done with one microscope objective, and the alignment marks for the X and Y directions cannot be seen in the same field for view. The theta correction is done first by aligning a mark on one side of the template, and then viewing a mark on the other side, and adjusting θ to compensate for misalignment. This is repeated until both marks are aligned. The X and Y alignment is done with cross-in-box marks and Vernier marks (see Figure 3.4). In Figure 3.4, both the ACTIVE and POLY layers are shown. The darker features are the ACTIVE pattern and the lighter features are the POLY pattern. The Vernier marks are for fine alignment in one direction only. The error in alignment can be measured after imprinting, by determining which marks are aligned on the Vernier scale. The upper and lower scales are placed with different spacing. When the center marks are aligned, the error in the direction of the scale (left to right in this case) is less than 0.25 microns. When the marks one-from-center are aligned, the error is 0.25 microns. When the marks two-from-center are

aligned, the error is 0.5 microns, and so-on. Rough alignment in X and Y is done with the cross-in-box marks, and the fine alignment is done with the Vernier marks. Once one direction is aligned, the mark for the other is viewed, but unfortunately the X and Y motions are coupled, so alignment can be lost in one direction while adjusting the other.

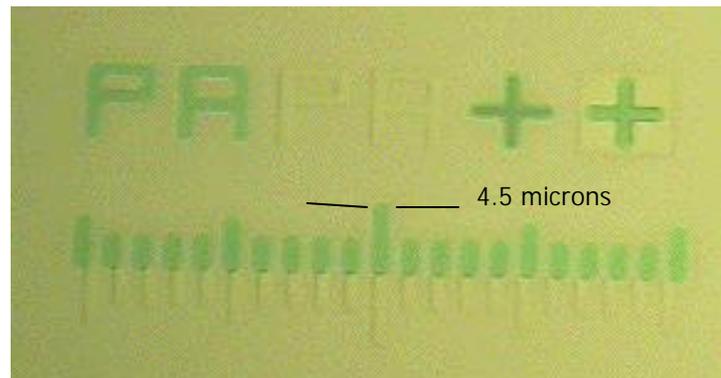


Figure 3.4. Microscope image of an aligned imprint above the active pattern, showing the alignment marks.

3.5 RESULTS

3.5.1 Uniformity of imprints

The uniformity of the aligned imprints can be judged visually, based on color variations and fringes, as well as with measurements of the cross-sections with a SEM. Figure 3.5 shows images from photographs of a planarization imprint on the ACTIVE patterned wafer, and the same wafer after it was imprinted upon with the POLY patterned S-FIL template. The upper/left image shows the planarization imprint covering about one half of a die. It has concentric color variations, suggesting a domed or cupped shape. Judging by the color

variations it is about 300nm thick. The lower/right images shows the same wafer and planarization imprint with the POLY patterned imprint on top of it. The imprint covers the 1” square area of the template, and shows horse-shoe shaped bands of color variation. The bands represent approximately 200-250nm change in thickness from dark band to dark band. The distance between these bands on the imprint is about 4 mm in the area of the planarization imprint. This suggests a change in thickness of 50 nm/ mm in residual layer thickness, if the planarization layer is ignored. The etch barrier surrounds the planarization imprint and is thinner above the planarization imprint than next to it. This will increase the variation in the etch barrier thickness, but will significantly decrease the etch barrier residual layer thickness above the planarization imprint. The alignment achieved of this imprint is shown in the next section.

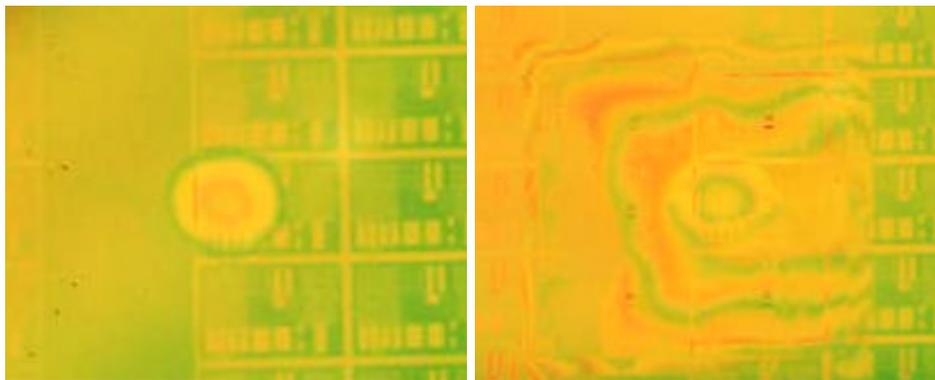


Figure 3.5. Images of a wafer shown for thickness uniformity approximation with planarization imprint (left) and subsequent POLY patterned imprint.

Another aligned imprint was diced and examined with the SEM. The layers of the etch barrier and planarization layers are clearly separate and show

the thicknesses of the respective layers. These images are shown in Figure 3.6. The layer of XCHA shows sporadic ductile failure, which sometimes makes it hard to see the upper XCHA/Barli interface. The upper image shows the etch barrier and planarization layers with thickness of 125 nm and 825 nm, respectively. The lower image shows the etch barrier layer and planarization layers with thickness of 115nm and 825nm. The difference in thickness of the layers is near the approximate error in measurement. Although the thickness comparison is over a short distance, it suggests a gradual change in the layer thicknesses. Although this region is small in comparison with the die and the template, it is big enough to include a device. With better residual layer control, a similar variation in thickness will span greater areas and lead to greater throughput.

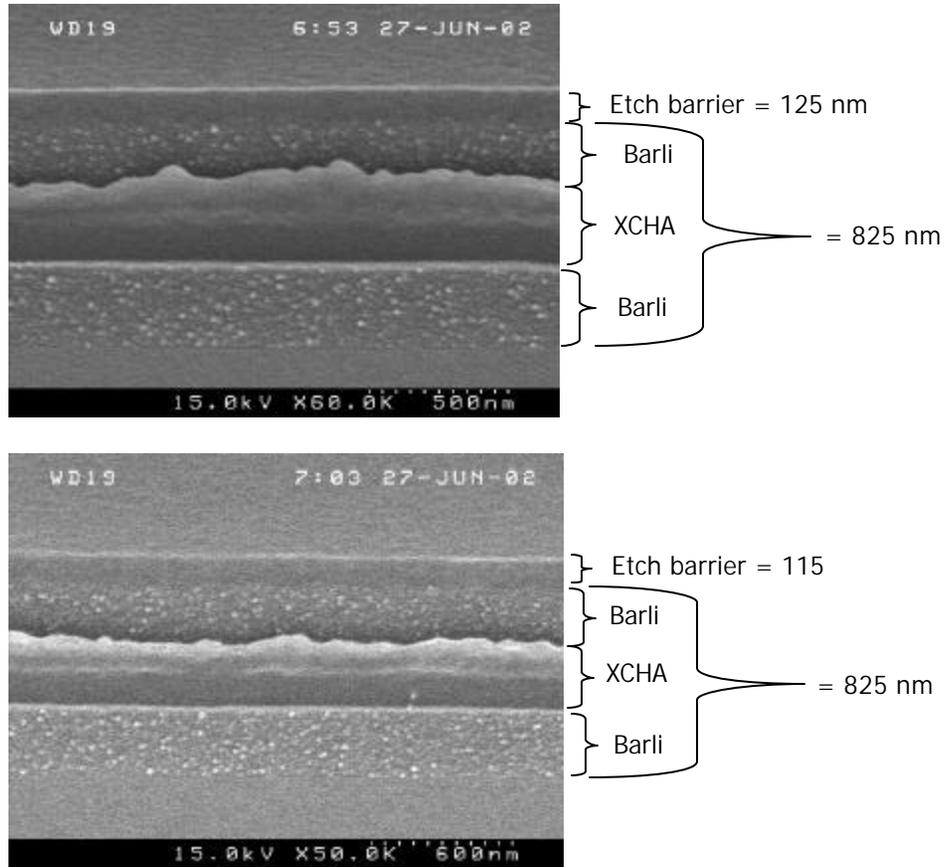


Figure 3.6. Cross-section SEM of an imprints in two locations 0.25 mm apart, showing little difference in etch barrier residual layer and planarization layer thickness.

The thicknesses of imprints and planarization layers were measured on other wafers. The etch barrier residual layers and planarization layers varied from 155 nm – 260 nm and 770 nm – 915 nm, respectively. This variation can be attributed to large variation in dispensed volume of monomer.

3.5.2 Alignment results

Sub-micron alignment in the X and Y directions was achieved using the OAM. The X and Y alignment error can be read from the Vernier alignment marks after the patterning imprinting process, by viewing the imprint through a light microscope. The X and Y alignment marks from the center die of the imprint shown in Figure 3.5 are shown in Figure 3.7. The Y-direction alignment mark (left) shows an error in alignment of about 0.25 microns. The X-direction alignment mark (right) shows an error in alignment of about 0.5 microns. Aligned gates from this imprint are shown in Figure 3.8. The alignment was acceptable across the imprint – on the adjacent die, the X-direction error was 0.5 microns, and the Y-direction error was 0.25 microns.

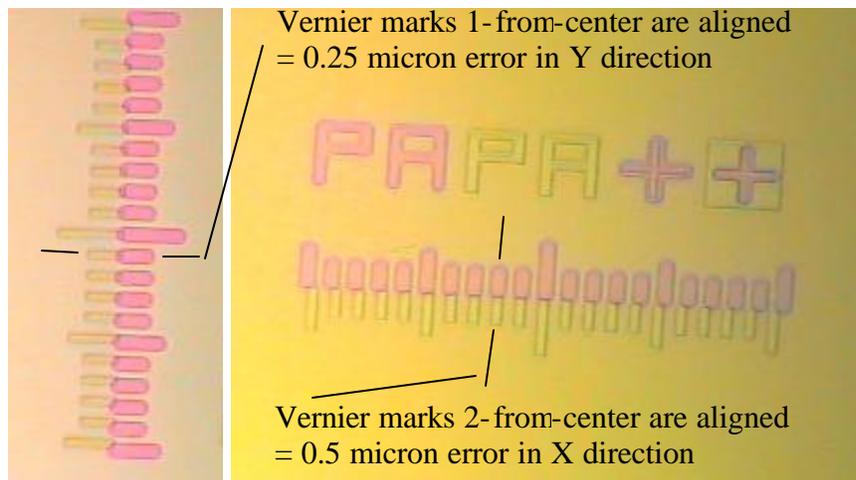


Figure 3.7. Microscope images showing the alignment marks from imprint shown in Figure 3.5.

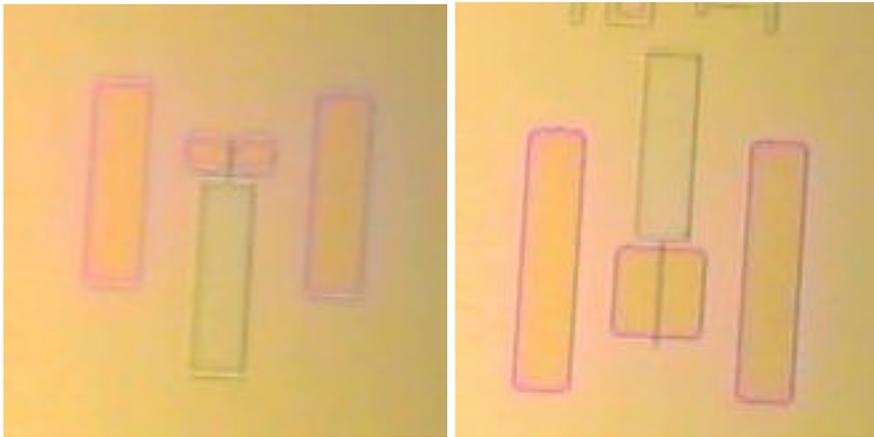


Figure 3.8. Microscope images showing imprinted gates structures aligned over active areas from imprint shown in Figure 3.5.

Chapter 4: Etching

4.1 INTRODUCTION

After the pattern to be transferred into POLY has been imprinted above the planarization layer, it must be etched into the POLY layer (see Figure 1.11 for designation of the POLY layer). This is achieved by etching the various of films with a series of different etch processes. The first two etching processes are discussed in this thesis: the halogen “break-through” etch which removes the residual layer of the S-FIL imprint, and the oxygen “transfer” etch which transfers the pattern through the planarization layers. This chapter will give a brief background on reactive-ion etching, describe the etching needed for S-FIL, discuss the problem of micro-masking, give critical dimension variation data for both the halogen and oxygen etches, and some comparisons of the observations to the prediction of what thickness variations will allow good pattern transfer, and developed a strategy for etching based on the planarization and imprinting achieved.

4.2 REACTIVE-ION ETCHING

Reactive-ion etching (RIE) is a process that is commonly used in the microelectronics industry to anisotropically, and often selectively remove material from the surface of a substrate. Anisotropy is defined as the vertical (normal to the macroscopic surface) etch rate divided by the horizontal etch rate. Anisotropy is needed to transfer pattern features through films without sacrificing the feature

width. This is especially important in transferring the high-resolution patterns used in the state-of-the-art microelectronic devices today. Selectivity is defined as the etch rate of one material divided by the etch rate of another. A high selectivity allows thin resists to withstand the etching needed to transfer the resist pattern through a thicker film of the other material. RIE can be both anisotropic and selective, because it uses both physical and chemical processes to remove material. The physical processes of the ion bombardment of the surface allow for the anisotropy, and the variety of chemical reactions allow for the selective material removal. A detailed discussion of plasma etching is provided by Mucha, Hess, and Aydil [Thompson, Willson, and Bowden 1994].

RIE is achieved when a plasma is created in a low-pressure gas, which reacts with a substrate to form gaseous byproducts. The plasma is an electrically conducting gas, which has loose electrons, ions, and neutral species. It is generally formed by applying an electric field to a volume of gas [Thompson, Willson, and Bowden 1994]. In etching chambers, the substrate is normally set on a plate that acts as a lower electrode, and the plasma is created above it. The reactive gases are fed into one part of the chamber and are pumped out of the other side. The measured characteristics of the RIE process are the etch rate, uniformity, anisotropy, selectivity, and radiation damage. These are influenced by key plasma properties, which in turn are determined by the power, pressure, gas flow rate, gas composition, excitation frequency, reactor geometry, and reactor materials [Thompson, Willson, and Bowden 1994]. Other process parameters can include the substrate temperature and the bias electric potential.

RIE is notoriously complex and empirical in nature, and considered by many to be a black art.

Some trends for RIE can be deduced that are useful in RIE process work. Increased power increases the ion density, which will increase the etch rate and can decrease anisotropy. Increased gas flow rate will increase uniformity, because an increased flow rate will decrease variation of the local gas species concentrations. Increased pressure will increase the etch rate and decrease the anisotropy. Increased DC bias will increase anisotropy and increase sputtering [Colburn 2001]. Lower wafer chuck temperature increases anisotropy [Jurgensen 1992].

There are a variety of etching systems, which vary in geometry, complexity, and cost. Some etching systems have additions that aid the processing further, such as interferometers for in-situ thickness and etch rate measurements, and spectrometers that detect gas species to determine when the material exposed to the plasma changes (for end-point detection).

The RIE tool in the MER used in this project is a PlasmaTherm 790 series. All of the etching reported in this chapter was done in this tool. Both the halogen and oxygen etches are done in a chamber that is supplied with CHF_3 and O_2 . A schematic of the system is shown in Figure 4.1. The process parameters that can be varied are the gas flow rates, the RF power, and the pressure.

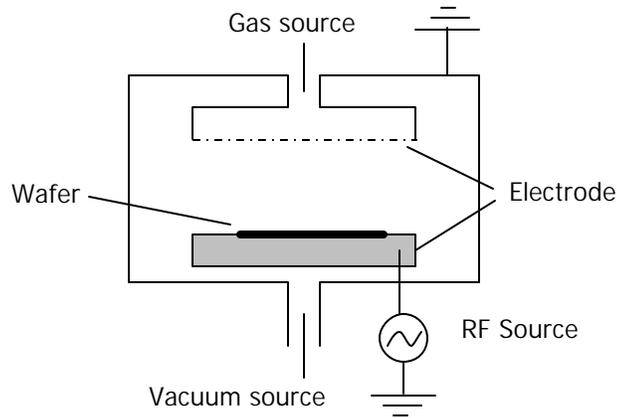


Figure 4.1. Schematic of the reactive-ion etching system used.

4.3 BACKGROUND ON THE ETCHING NEEDED FOR S-FIL

The additional etching steps needed for the integration of S-FIL into the MOSFET fabrication process are fundamentally the same as the typical etching needed for most S-FIL processing. The halogen “break-through” etch is used to remove the residual layer of the S-FIL imprint. The standard halogen etching conditions used for this thesis work are: CHF_3 with a flow rate of 40 sccm (standard cubic cm per minute), O_2 with a flow rate of 2 sccm, pressure of 20 mTorr, and RF voltage of 450V. These settings were adapted from previous etch work, except for the oxygen flow rate which was reduced after experiments aiming to reduce post-etching residue. When this etching is completed, all of the Si-containing etch barrier is removed from on top of the planarization layer, except for part of the layer that is the POLY pattern. This exposes the parts of the surface of the planarization layers that need to be removed. The oxygen transfer

etch transfers the pattern through the planarization layers by removing the parts of the planarization layer that are not protected from the etching plasma by the S-FIL etch barrier. It is called an amplification step, because it amplifies the aspect ratio of the features. The taller features can generally allow the etching of thicker films without the mask being completely consumed by the etch. The standard oxygen etching conditions used for this thesis work are: O₂ with a flow rate of 8 sccm, pressure of 8 mTorr, and a RF voltage of 300 V. Figure 4.2 shows the process flow of the etching needed for the S-FIL integration into the Si-Ge-C MOSFET fabrication process. As with the similar figures shown previously, the schematics in Figure 4.2 represent cross-sectional views of the wafer not to scale. The flow begins with the POLY patterned imprint of possibly varying thickness. The feature height is about 230 nm, because of the shrinkage from curing. The pattern is transferred from the halogen and oxygen etches. The etching as discussed in the scope of this thesis is done when the oxide hard mask surface is exposed with the planarization layer that was masked by the POLY pattern remaining on top of it. In this state the wafer is ready for the etching of the hardmask.

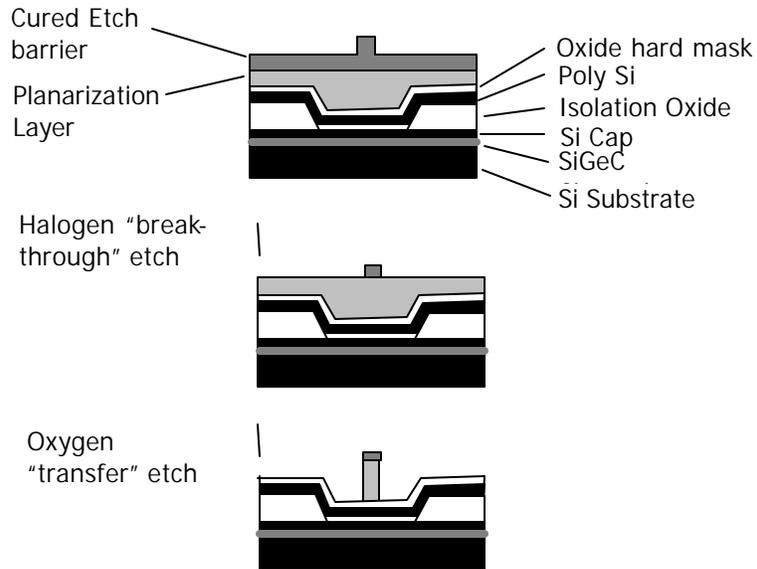


Figure 4.2. Etch processes needed for S-FIL integration into the MOSFET fabrication process.

Figure 4.3, 4.4, and 4.6 show SEM images of the etch transfer of a dot pattern. The samples shown in these figures were etched on a graphite chuck (rather than aluminum). The significance of this is explained later in this chapter. All the SEM images shown in this chapter were taken with the sample tilted 60 degrees from the horizontal, so that the sample is 30 degrees away from being viewed at a purely cross-sectional view. All of the samples were sputter coated with a Au/Pd coating to reduce charging and facilitate good imaging. The upper image shows the cross-section and top surface of an imprint with a single dot in the center. The top half of the image is the surface of the imprint and the bottom half of the image shows the cross-sectioned residual layer on a thicker layer of Barli (on a silicon dioxide coated wafer). The dot is actually in the shape of a

tower, with a small bump next to it (on its left side). The small bump was an imaging defect created in the making of the template; it is a feature on the template that is imprinted along with the desired dot-tower. The dot-tower is approximately 200nm tall and the small bump next to it is less than 100 nm tall. Figure 4.3 shows the surface of the Barli film with the dot-tower sitting on top of it. A little bump is next to the dot-tower (on its right side) similar to the little bump seen in the upper image of the un-etched imprint. The surface of the Barli is granular, much more so than an unetched Barli film shown with the same magnification (see Figure 4.5). This surface roughness is not likely due to the Au/Pd coating used for the SEM, because the sample was coated with a similar amount to the sample shown in Figure 4.3, which does not have the roughness. This roughness is likely due to the uneven etching of the (organic) Barli with a etch process that is used to etch silicon dioxide containing films. The dot-tower in Figure 4.4 also shows the vertical ridges on the vertical surfaces of the feature. With these process conditions, these vertical ridges grow with increasing etch time, and suggest that material is being deposited onto the vertical surfaces (while it is being removed from the horizontal surfaces). Figure 4.6 shows a dot-tower that has been halogen etched and then oxygen etched. The bases and tips of other towers are also visible. The tips of the towers are the remains of the etch barrier dot-towers. The surface of the oxide below the Barli is now exposed, showing some small roughness. There is similar roughness the sample with the wet-etched oxide topography shown in Figure 1.4. The widths of the etched tower shown in Figure 4.6 is significantly less than the towers shown in Figure 4.3 and 4.5. This

is primarily due to the anisotropy of the oxygen etch process used, but cannot be used with confidence, because the dot-tower shown in Figure 4.3 was not etched to be the dot-towers shown in Figures 4.5 and 4.6. The dot-towers were imprinted in an array and are not all the same width. This is discussed further in Section 4.5.

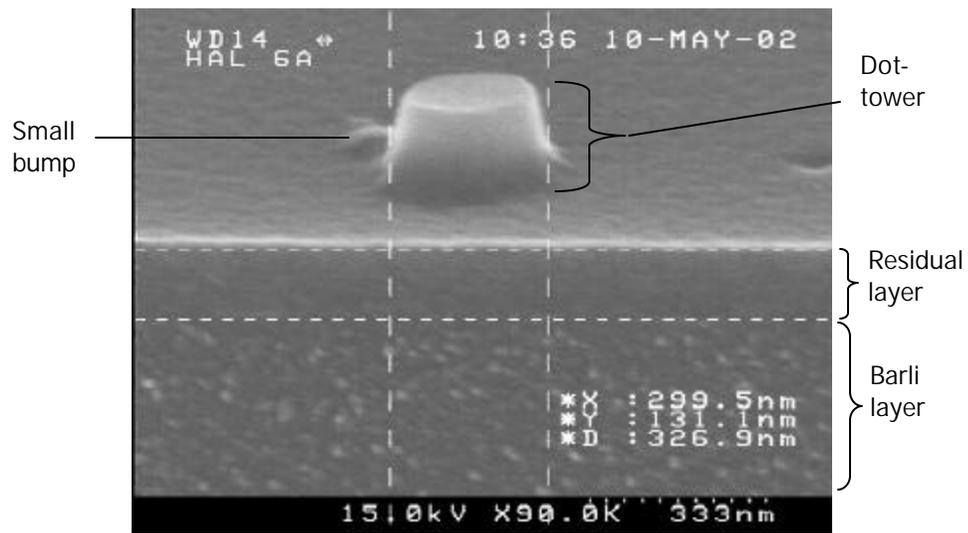


Figure 4.3. SEM image of an imprinted dot-tower (unetched).

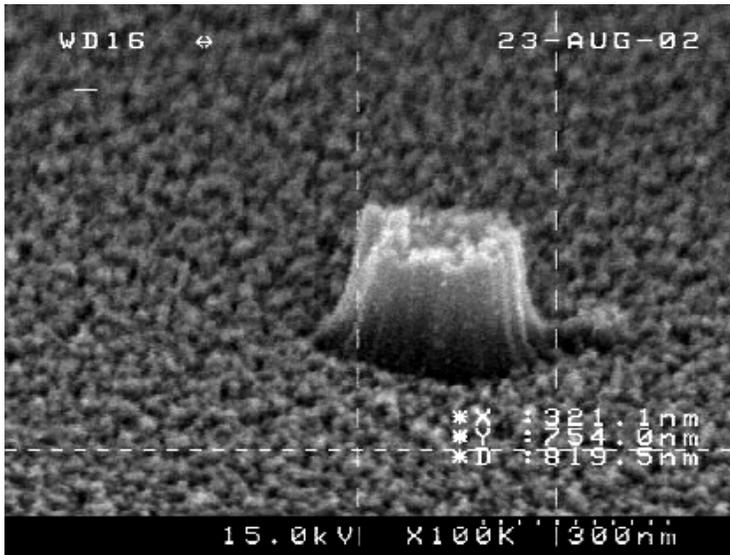


Figure 4.4. SEM image of an imprinted dot-tower after a break-through etch.



Figure 4.5. SEM image of a Barli film (unetched).

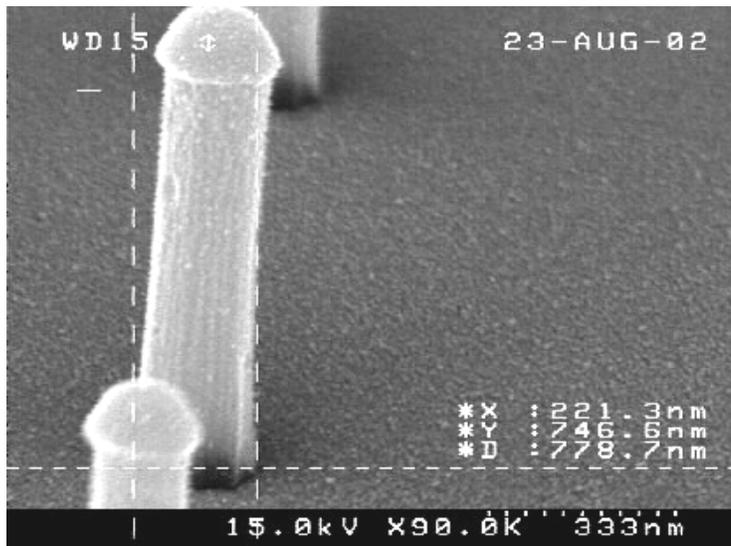


Figure 4.6. SEM image of an imprinted dot-towers after the break-through etch and the oxygen etch.

4.4 GRASS PROBLEM

Unlike the etched samples shown in the SEM images in Figures 4.4 and 4.6, most of the etching done for this thesis was plagued with a residue or “grass” problem. This grass is the product of micro-masking of the film being etched. When a micro-masked film is etched, the parts of the film directly under the particulates doing the micro-masking are not etched nearly as fast, causing a non-uniform film, and eventually grass-like structures. The diameters of these structures vary, but are generally about 20-40 nm, and with an approximate spacing of 40 nm. The size and amount of the grass formed generally increases with etch time. There was micro-masking observed after each of the subsequent etches (halogen, oxygen, and etching of the underlying oxide film). Examples of the grass problem are shown in Figures 4.7 and Figure 4.8. The sample etched in

these two figures was diced after the halogen etch. One was put away to be viewed in the SEM (shown in Figure 4.7), and the other was oxygen etched (shown in Figure 4.8). Figure 4.7 shows SEM images of imprinted dot patterns after the standard halogen etch mentioned previously. The residual layer thickness of the imprint was 175 nm, and the sample was etched for 5 min (at approximately 40 nm/min). There is a uniform roughness across the film, except for the space immediately next to (60-120 nm) the dot-tower features. The roughness is similar to the roughness shown in Figure 4.4, but the roughness in Figure 4.4 does not change with proximity to the feature (also indicating that the roughness is caused from a different source). Also, the sample that was halogen etched and shown in Figure 4.4 was diced and the oxygen etched to produce the sample shown in Figure 4.6, which has no grass. The grass shown in Figure 4.8 will mask the oxide during the following etching steps, and is completely unacceptable – devices will not functionally properly (if at all) if made with similar processing.

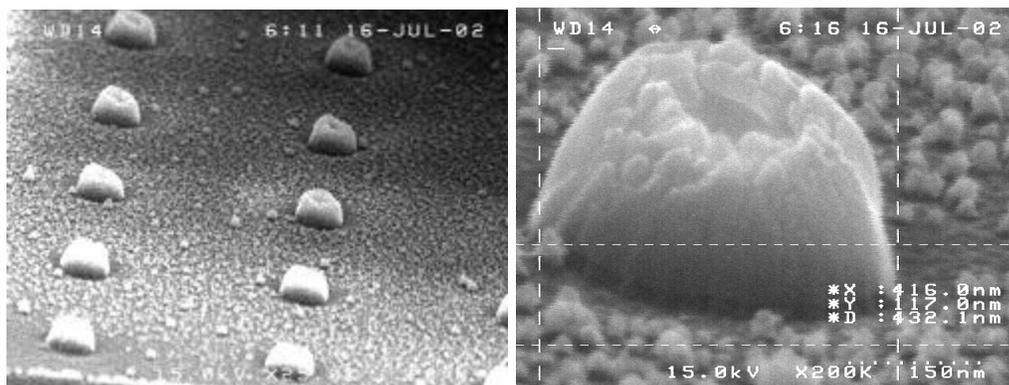


Figure 4.7. SEM images of imprinted dot patterns after the halogen etch (July17 images 1 and 2).

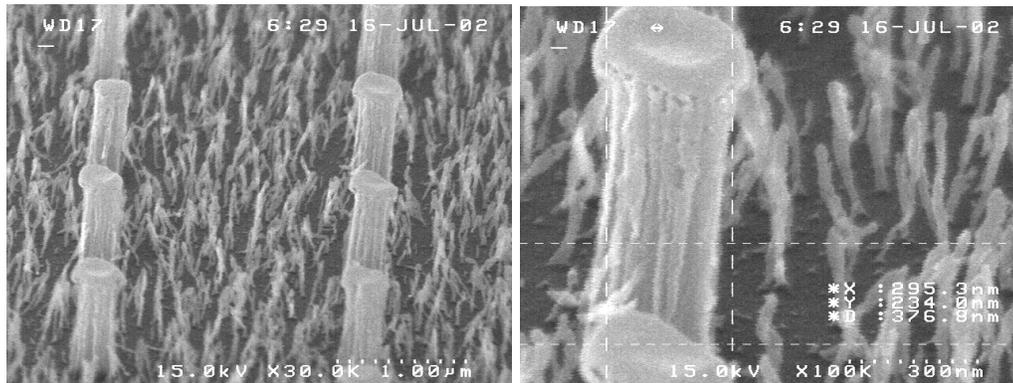


Figure 4.8. SEM images of imprinted dot patterns after the halogen etch and oxygen etch.

Residues like the ones shown in Figures 4.7 and 4.8 have been documented by other researchers. Residues are a problem with silylation-based processes for surface imaging [Sheats and Smith 1998]. The DESIRE process is a multilayer resist scheme that silylates (adds silicon containing molecules to) an exposed (patterned) resist on top of an organic planarization layer. These residues are caused by unintentional silylation of the oxygen etch mask layer and sputtering and redeposition of materials. This can be improved by optimizing the silylation and bake conditions to improve the selectivity of the silylation step, or by using a non-selective etch step [Sheats and Smith 1998]. Residues can also come from sputtering of the exposed electrode, such as the wafer chuck in the PlasmaTherm 790 series etcher [Thompson, Bowden, and Willson 1994]. More specifically, aluminum wafer chucks have been shown to cause grass-like problems [Palmour 1987] and [Rangelow et al. 1986]. The solution suggested is to use a graphite wafer chuck instead of an aluminum one.

Suspecting that the etch barrier material was not being completely removed by the halogen etch, samples were halogen etched longer than necessary. Afterwards they samples were diced in half, and one half was oxygen etched to see if the pattern transferred well. This over-etching did not solve the grass problem.

Next, suspecting that the mixture of gasses used during the oxygen etch was not removing the etch barrier uniformly, samples were halogen etched with varying oxygen flow rates. The flow rate of CHF_3 was held constant at 40 sccm and the oxygen flow rate was varied – 2, 5, and 10 sccm. Increasing the flow rate of oxygen increased the etch rates, so samples were etched for different times to etch the samples the same thickness. This did not solve the grass problem, but the sample with the oxygen flow rate of 2 sccm appeared to have the least grass, even compared to the samples that were etched for similar thicknesses (and less time). All of the etching afterwards was done with 40 sccm of CHF_3 and 2 sccm of O_2

Next, suspecting that the grass was silicon-dioxide containing material, HF containing 6:1 buffered oxide etch (BOE) was used to try to strip the residue after the halogen etch, mid-way through the oxygen etching process, and after the oxygen etching process. The BOE removed a significant amount of the grass, but did not work completely to solve the problem.

Next, suspecting that the grass was caused by the aluminum wafer chuck, a wafer with a layer of Barli was oxygen etched (with no imprint). The Barli should be able to be completely removed by oxygen etching. Multiple layers of Barli were spun onto a bare Si wafer (with native oxide) to create a film 870 nm

thick. The wafer was diced into different pieces and oxygen etched for different times; to see how the film looked before, at, and after the etching time needed to completely remove it. The etching conditions used were 8 sccm of oxygen, 6 mTorr, 300V and produce a vertical etch rate of about 100nm/min. The sample was etched for 10.75 minutes. Even after minutes of over-etching, there was a lot of grass remaining on the wafer (see Figure 4.9). A similar sample was taken and given to researchers to perform a X-Ray Photoelectron Spectroscopy (XPS) scan. This scan showed an approximate 6% atomic concentration of aluminum on the sample surface (see Figure 4.10). This data was suggested buying a graphite chuck for the etcher.

After a graphite chuck was installed into the etcher, samples were halogen and oxygen etched, and showed no grass (see Figure 4.4 and 4.6). There is a tremendous difference in the residue shown in Figures 4.8 and 4.9 (etched with the aluminum chuck) and the roughness shown in Figure 4.6 (etched with the graphite chuck). The residue shown in Figures 4.8 and 4.9 is consists of strands of material over 100 nm long which are clearly not a part of the substrate. The surface of the substrate shown in Figure 4.6 appears grainy with a mean grain size of approximately 10 nm. This difference suggests that the aluminum chuck was the root cause of the residue problem, and the etching processes can be done without micro-masking when the graphite chuck is used.

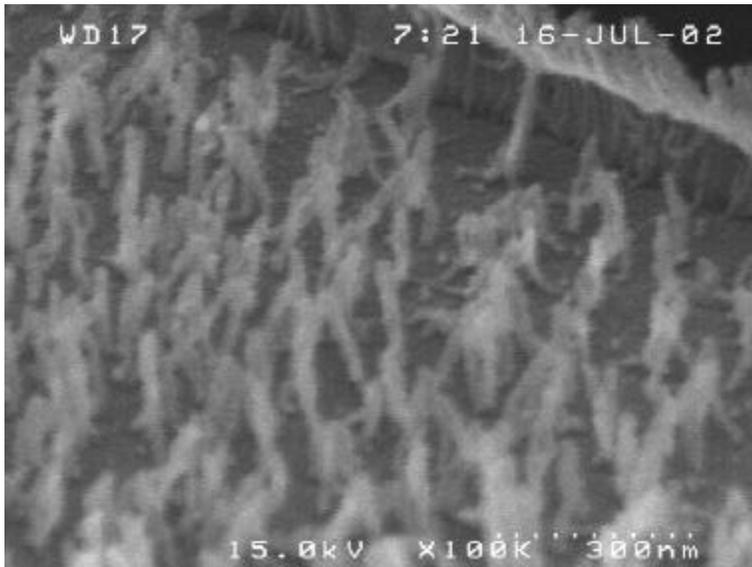


Figure 4.9. SEM image of a wafer with Barli that was oxygen etched, showing grass.

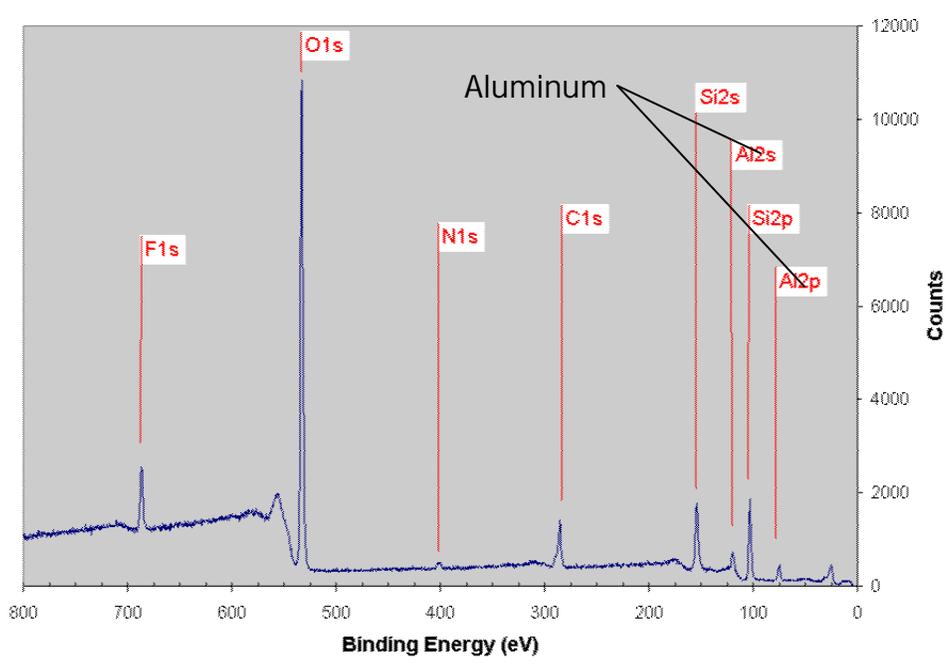


Figure 4.10. XPS data showing 6% atomic concentration of aluminum on the etched Barli sample.

4.5 CD LOSS MEASUREMENT

One of the important characteristics of an etch process is control of the critical dimension (CD). A decrease in the width of the normally smallest dimension of the pattern being transferred is often seen. An ideal method of measuring the CD loss would be to measure the width of a feature (without affecting it), perform the etch process, and then re-measure the same feature. This was not a viable technique, because the resolution needed to measure CD losses of less than 100 nm was not possible without coating the sample and viewing it in the SEM. This coating prevents the sample from being processed further. Samples were viewed in a LEO SEM with 1kV accelerating voltage, and 3 mm working distance, and 300 nm features were too blurred to measure easily. An alternative to viewing the same feature before and after processing is to use different features that approximately have the same widths before the processing of interest. The width of the feature on the sample that did not undergo the process of interest is the approximation of the pre-process width of the feature on the sample that did undergo the processing.

The dot-tower pattern was used to make CD measurements (see Figure 4.11 and 4.3). The dot-tower pattern is a square array with two-micron spacing between dots. Figure 4.11 shows an imprint of the dot-tower pattern that has been diced. There is some residue near the edge of the diced edge, and some dot-towers have been broken off. Each dot-tower is approximately 300 nm wide and 200 nm tall (depending on how it is measured). The measured widths of 25 dot-towers across 10 mm vary by 40 nm with a standard deviation of 12 nm, but

locally the widths of the dot-towers varied less. The widths of nine dot-towers were measured and averaged to make each measurement for a CD loss (18 dot-towers measured for each CD-loss value). Nine towers were measured on each of 20 samples. The standard deviation for each group of 9 measurements was calculated. The average of the standard deviations of the 20 groups of measurements was 10 nm, with a standard deviation of the standard deviations to be less than 3 nm.

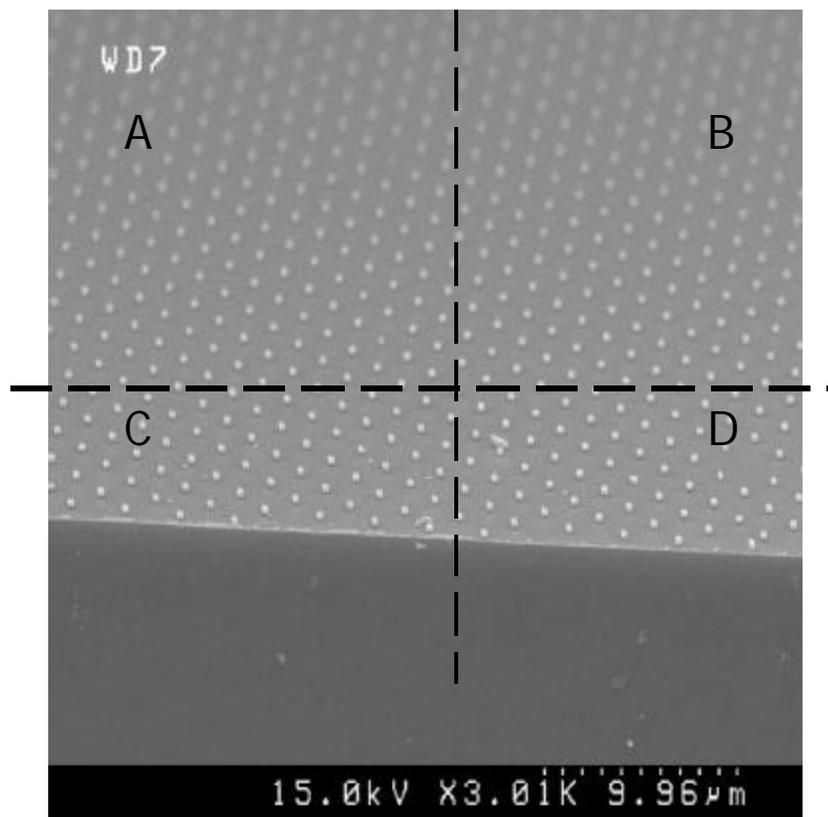


Figure 4.11. SEM image of the dot-tower pattern with lines showing how a wafer could be diced for CD loss measurement.

The CD loss measurement was made by approximating the pre-etch widths of a dot-towers with the widths of dot-towers on a part of the imprint that was immediately next to the towers that were etched. The procedure used also gives some verification that the etching process of interest was good, by etching a part of the sample with the same conditions as those measured for CD loss, as well as etching the sample with the next subsequent etch step. When determining the CD loss of the halogen etch step, one part of the sample was oxygen etched. When determining the CD loss of the oxygen etch step, one part of the sample was etched with a silicon oxide etch. The scheme for CD loss measurement for the halogen etch is as follows:

- ? A wafer is imprinted with the dot-tower pattern
- ? The wafer is diced, splitting the dot-tower pattern into two halves; one containing parts A and B (see Figure 4.11) and the other part containing parts C and D
- ? The half with A and B is diced again, splitting the half into parts A and B
- ? Part A is put away, the dot-towers on the corner will be measured
- ? The half with C and D is diced again, (with the dice as close as possible to where the half with A and B was diced) splitting the half into parts C and D
- ? Parts B, C, and D are halogen etched the desired time
- ? Part B is put away, the dot-towers on the corner will be measured and compared to those on part C
- ? Part C is put away, the dot-towers on the corner will be compared to those on Part B
- ? Part D is oxygen etched for the desired time
- ? Part D is put away, the dot-towers on the corners will be inspected
- ? The widths of nine dot-towers are measured on each of the parts A and B
- ? The difference in the average of the widths is the CD loss (or gain)
- ? Parts B and C are compared to see if they received similar processing
- ? Part D is inspected to see if the etch processing done for the CD loss measurement was good enough to transfer the pattern

The CD loss measurement for the oxygen etch was similar that of the halogen etch, except the whole wafer was halogen etched before it was diced (and part A was put away). In addition, part D was etched with a silicon dioxide-etching process.

The results from the CD loss measurements are shown in Figure 4.12. Eight CD loss measurements were taken for the oxygen etch and ten were taken for the halogen etch. The etch rate of Barli and cyclohexal acrylate were found to both be 100nm/min with the standard oxygen etching, so a 600 nm layer of Barli was used in each of the oxygen etched samples.

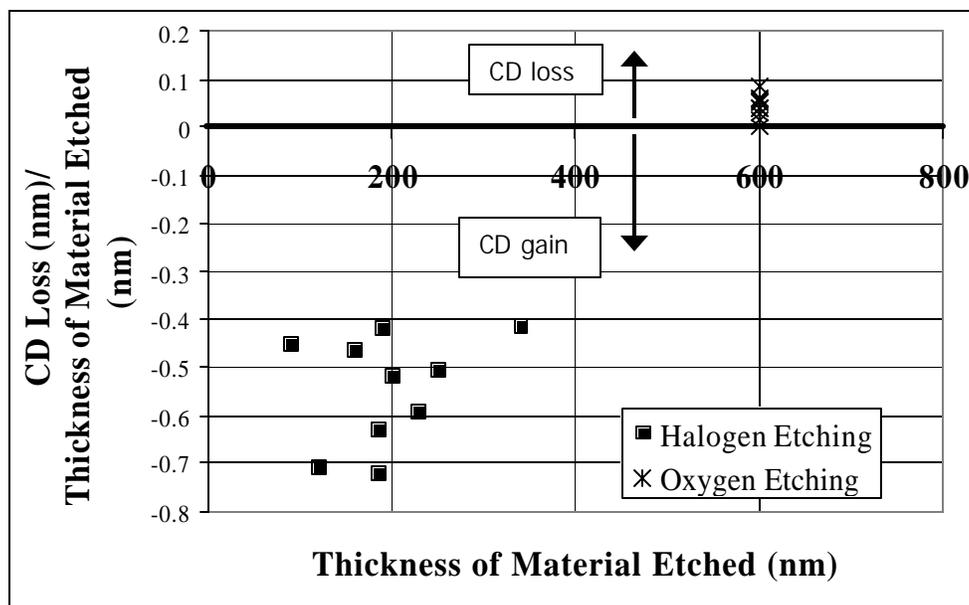


Figure 4.12. CD loss/Thickness of Material Etched for the halogen and oxygen etch processes used.

The oxygen etching conditions were 8 sccm of O₂, 8 mTorr, and RF voltage of 300 V. All of the samples that were oxygen etched were 600 nm thick

layer of Barli, and were etched so that the layer was over-etched by approximately 100 nm. The positive values of CD loss indicate that the oxygen etching process decreased the CD of the features. The CD loss for the oxygen etched samples varied from 0 to 0.1 nm of CD loss for every nm of Barli etched, with an average of less than 0.05 nm of CD loss for every nm of Barli etched. This corresponds to an approximate anisotropy of 20 for this process. Features etched through a 600 nm thick planarization layer should have approximately 30 nm of CD loss.

The halogen etching conditions were 40 sccm of CHF_3 , 20 mTorr, and RF voltage of 450 V. The sample that was halogen etched had residual layer thicknesses that varied from 100 nm to about 350 nm. All of the samples that were halogen etched were etched so that the residual layer was completely removed, with approximately 50 nm of over-etch. The negative values of CD loss indicate that the halogen etching process increased the CD of the features. All of the samples had significant CD gain from the halogen etching process, varying from 0.4 to 0.7 nm of gain for every 1 nm of etch barrier etched through, with an average of 0.55 nm of gain for every 1 nm of etch barrier etched through. This may be attributed to the deposition rate of the etch barrier on the vertical surfaces of the features was greater than the removal rate of the etch barrier on the vertical surfaces of the features.

All of the CD loss measurements were done before the aluminum chuck was replaced with the graphite chuck. Grass was present in all of the samples, and may have influenced the CD loss measurements. The presence of the grass would decrease the local etch rates by an unknown amount, relative to a grass-free

sample. Without the presence of grass, the amount of the material being etched exposed to the etching gas dramatically decreases when the layer being etched is completely removed. The lack of material being etched should slightly increase the etch rate, because of the lack of chemical loading. With this theory, the grass presence should dampen the effects of over-etching the samples on CD loss.

4.6 PREDICTED ETCH TRANSFER

The estimations of the minimum allowable flatness used in Chapter 2 to define the planarization requirement can be used to predict the allowable variation in the etch barrier residual layer. The parameters and values used are listed in Table 4.1. The maximum allowable depression depth ' v_{max} ' was shown to depend on the imprinted feature height ' f ', the etched surface roughness (and approximate overetching needed) ' r ', the minimal mask of the etch barrier needed ' m ', and the variation in the residual layer thickness ' R_v ':

$$v_{max} \propto f \cdot r \cdot m \cdot R_v$$

where ' f ' is 233 nm, ' r ' is 20 nm. ' m ' was estimated to be the planarization thickness ' p ' (including the 250 nm feature height) divided by the oxygen etch selectivity of the etch barrier to organics, ' s ', plus the surface roughness after etching ' r ':

$$m \propto \frac{p}{s} + r$$

For ' p ' equal to 950 nm, ' s ' equal to 12, and ' r ' equal to 20 nm, ' m ' is equal to 99 nm. ' v_{max} ' can be assumed to be 35 nm with the Barli-XCHA-Barli planarization method demonstrated. The allowable variation in residual layer thickness ' R_v ' is

equal to the range of residual layer thickness that will transfer the imprinted pattern without pattern loss:

$$R_v \approx f + r + m + v_{\max}$$

With the values mentioned above and listed in Table 4.1, the range of residual layer thickness that will transfer the imprinted pattern without pattern loss is equal to 79 nm.

Parameter	Definition	Value used
f	Imprinted feature height	233 nm
r	Etched surface roughness and over-etching needed	20 nm
p	Planarization layer thickness (including the 250 nm trench depth)	950 nm
s	Etch selectivity of etch barrier to organics	12
v_{\max}	Maximum variation in the planarization layer surface (depression depth of planarization layer)	35 nm

Table 4.1. Parameters used to calculate the range of thickness of residual layer that will transfer imprinted patterns.

If the thickness of the residual layer is measured (outside of a trench) to be ‘R’, the time of the halogen etch can be determined (with an assumed etch rate) based on an adjusted distance need to etch ‘A’. ‘A’ is larger than ‘R’ because of the overetching needed, and is represented by v_{\max} and r. Assuming no error in the measurement of ‘R’ or the etch rate, ‘A’ can now be estimated:

$$A \approx R + v_{\max} + r$$

With this value, the area of the etch barrier imprint that has a thickness less than 'R' and greater than 'R' minus 'R_v' should be transferred with good pattern retention.

The change in CD through etching can be predicted with given residual layer and planarization layer thicknesses, and demonstrated etch rates. Assuming a residual layer of 200 nm, a planarization layer of 950 nm (including the 250 nm feature height), halogen etch CD gain of 0.55 nm/nm of etch barrier etched, and oxygen etch CD loss of 0.05 nm/nm of planarization layer etched, the CD will be increased by 60 nm by the combination of the etching processes.

Chapter 5: Conclusions and Future Work

5.1 CONCLUSIONS

5.1.1 Overview

This research has demonstrated that S-FIL and accompanying processing may be used for planarization, and alignment and imprinting over planarized topography, and pattern transfer with RIE without “grass”-like residue. Further development is required before the S-FIL process can be used to fabricate MOSFETs, as well as other devices. Conclusions specific to the processes of planarization, alignment and imprinting, and etching are discussed below.

5.1.2 Planarization

The S-FIL process can be used to planarize topography by using Si-free organic monomers and a featureless (flat) S-FIL template [Colburn, Grot, and Choi et al. 2001]. With the combination of spin-coating and a planarizing S-FIL imprint, the planarization needed for the S-FIL process to be used in the fabrication process of MOSFETs can be achieved. The planarization of 240 nm deep topography was shown with planarization layers of combined thickness of less than 650 nm; 10 μ m wide trenches were planarized to 10-30 nm (96-88%), and 150 μ m wide trenches were planarized to 20-40 nm (92-83%). This difference was due to the difference in planarization achieved by the first spun Barli layer. The narrow trenches were planarized more by Barli, and the degree

of planarization is determined by the partially planarized topography. Experimental results showed that spin-coating planarized topography to varying degrees.

Cyclohexyl acrylate (CHA) was used to perform imprint planarization. It was found that a cross-linking agent should be used when planarizing with CHA. There was considerable loss of planarization when Barli was spun onto the CHA imprint, whereas there was no loss of planarization with the cross-linking solution (XCHA), which suggests solvent interaction.

5.1.3 Imprinting and Alignment

The S-FIL overlay machine can be used to imprint and achieve sub-micron layer-to-layer alignment over the topography planarized with the Barli-XCHA-Barli planarization layers. The alignment required for the device demonstration was $\pm 2 \mu\text{m}$. The thicknesses of etch barrier imprints over the underlying transfer layer composed of Barli-XCHA-Barli planarization layers were measured with the SEM. The etch barrier residual layers and planarization layers varied from 115 nm – 260 nm and 770 nm – 915 nm, respectively. These measurements were performed over multiple imprints. This variation can be attributed to large variation in the dispensed volume of monomer solutions. This variation is tolerable if layer thicknesses are measured on a wafer-to-wafer basis. The residual layer thickness of an aligned imprint was shown to vary from approximately 115 nm to 125 nm over 0.25 mm. The difference in the thickness values measured is on the order of the noise of the measurement.

The combination of the residual layer and planarization layer thicknesses, and the small variation in residual layer thickness (over the limited area mentioned) is acceptable for the desired pattern transfer (over the limited area mentioned). Imprints that cover a larger area of the wafer and maintain similar small variation in thickness have to be achieved before allowing for the pattern transfer of a larger area of the template.

5.1.4 Etching

The aluminum wafer chuck used in most of the etch development was found to cause a micro-masking problem that caused an undesirable residue after etching. XPS data showed a 6% atomic concentration of aluminum on an etched sample. After replacing the aluminum chuck with a graphite chuck, etched samples showed no such residue.

A baseline etching process that can transfer imprinted images into the bilayer materials has been demonstrated (see Figure 4.6). The halogen etch process required to break through the residual layer of the imprinted material was shown to increase the widths of the features that were etched. All of the samples had significant CD gain from the halogen etching process, varying from 0.4 to 0.7nm of gain for every 1 nm of etch barrier etched through, with an average of 0.55 nm of gain for every 1 nm of etch barrier etched through. This may be attributed to the deposition rate of the etch barrier on the vertical surfaces of the features being greater than the removal rate of the etch barrier on the vertical surfaces of the features. The oxygen etch process was found to have an

approximate anisotropy of 20. Features etched through a 600 nm thick layer of Barli were found to have approximately 30 nm of CD loss.

The quality of the planarization achieved provides an area with a range of allowed residual layer thickness over which imprinted images can be transferred without any predicted loss of features. Similarly, using the measured etch rates of the break-through etch and oxygen etch, the change in CD can be predicted for the whole process.

5.2 FUTURE WORK

5.2.1 Improve the Alignment Scheme

The manual alignment scheme used needs to be improved. Having only one objective is tolerable, but having two that can simultaneously look at two alignment targets would greatly simplify the process. The template size may have to be increased to accommodate two objectives of reasonable size simultaneously. The alignment marks used were good for the required alignment in one direction only. The alignment marks for both of the X and Y-directions should be located on the patterns so that they are visible simultaneously with the one microscope objective used.

5.2.2 Decrease Barli Layer Thicknesses

The planarization scheme using the S-FIL imprint planarization and the spin-coated Barli may be improved. The thickness of the planarization layer should be minimized to minimize the CD loss during the oxygen etch, and allow

the pattern transfer from a larger area of the template. A thinner planarization layer thickness allows a thinner layer of the etch barrier to act as a mask, which allows for a larger range of residual layer thickness that will transfer the imprinted pattern without pattern loss. Other formulations of Barli with lower percent solids content (that result in thinner layers) may be used to decrease the total thickness. The higher solvent content would have greater potential to mix with the planarization imprint, but as the Barli used did not show any sign of mixture, a more dilute solution could work.

5.2.3 Exclude Spin-coating

The layers of Barli were used in a conservative effort to retain the Barli's good interfacial properties. It is possible that the layers of Barli are not needed. The subtraction of spin-coated layers would dramatically decrease the planarization thickness, greatly decrease the CD loss during the oxygen etch, and allow the pattern transfer from a larger area of the template (for the same reason mentioned in the previous paragraph).

The cross-linking cyclohexal acrylate solution may satisfy all of the requirements of the transfer layer. If the cyclohexyl acrylate solution is highly cross-linked, the etch barrier solution may only mix with it for an insignificant amount (<10 nm). If the planarization imprints do not adhere well to the SiO₂ hard-mask, perhaps an adhesion promoter could be used, or a thin layer of Barli could be spun before the imprint.

5.2.4 Decrease Planarizing Imprint Shrinkage

The planarization imprint material currently shrinks greater than 10% when it is cured. This directly decreases the quality of planarization achieved. Although this planarization is very good for the topography in this processing, less shrinkage would allow for better planarization over taller topography. Because the flatness of the surface of the XCHA imprint was about 20 nm, the flatness after the second Barli layer was near the level of noise in the measurement. With taller topography, the depressions in the XCHA surface will be proportionally deeper, and will not be so easily planarized by the second Barli coat. For this reason, the shrinkage during curing of the planarization imprint is a material property worthy of further optimization.

5.2.5 Materials Development

To further improve the S-FIL technology, the development of etch barrier materials should be continued and optimized for viscosity, etch selectivity and anisotropy, shrinkage during the curing process, adhesion characteristics, and strippability.

5.2.6 Etching Anisotropy

The halogen etching used increased the feature sizes. For good CD control, the etch process should be modified for greater repeatability and minimal CD change. The oxygen etching process should be optimized to decrease the CD loss. The use of lower pressures, possibly an inert gas, or another etching tool is

suggested. The process needs to be redeveloped on a state-of-the-art etcher to fully understand CD performance and repeatability as a function of process variables.

5.2.7 Improve Imprint Thickness and Uniformity

The imprinted thickness and thickness uniformity are critical for the imprinted pattern transfer. Machine modifications should be considered that allow for automated fluid dispensing. Control of the fluid volume and drop placement would help reach the desired minimal thickness, and improve the thickness uniformity. Other machine modifications should be made to allow for thin, uniform imprints, over the entire imprinted field.

5.2.8 Complete the Process

With further development, the S-FIL process can be integrated into the fabrication process of MOSFETs, as well as other device fabrication processes. The process of patterning Si-Ge-C substrates and performing all the MOSFET fabrication steps should be completed to allow electronic characterization. With further optimization, the device performance advantages and disadvantages specific to S-FIL can be investigated and compared to the competing lithography technologies.

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