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Template fabrication schemes for step and flash imprint lithography

T.C. Bailey[a], D.J. Resnick[b],*, D. Mancini[b], K.J. Nordquist[b], W.J. Dauksher[b],
E. Ainley[b], A. Talin[b], K. Gehoski[b], J.H. Baker[b], B.J. Choi[a], S. Johnson[a],
M. Colburn[a], M. Meissl[a], S.V. Sreenivasan[a], J.G. Ekerdt[a], C.G. Willson[a]

[a]*Texas Materials Institute, University of Texas at Austin, Austin, TX 78712, USA*
[b]*Physical Sciences Research Laboratories, Motorola Laboratories, MDFL508 2100 East Elliot Road,
Tempe, AZ 85284, USA*

Abstract

Step and flash imprint lithography (SFIL) is an attractive method for printing sub-100 nm geometries. Relative to other imprinting processes, SFIL has the advantage that the template is transparent, thereby facilitating conventional overlay techniques. The purpose of this work is to investigate alternative processes for defining features on an SFIL template. The first method considered using a much thinner (< 20 nm) layer of Cr as a hard mask. Thinner layers still suppress charging during e-beam exposure of the template and have the advantage that CD losses encountered during the pattern transfer through the Cr are minimized. The second fabrication scheme addresses some of the weaknesses associated with a solid glass substrate. Because there is no conductive layer on the final template, SEM and defect inspection are compromised. By incorporating a conductive and transparent layer of indium tin oxide on the glass substrate, charging is suppressed during inspection and the UV characteristics of the final template are affected minimally. Templates have been fabricated using the two methods described above. Features as small as 30 nm have been resolved on the templates. Sub-80 nm features were resolved on the first test wafer printed. © 2002 Elsevier Science B.V. All rights reserved.

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1. Introduction

Step and flash imprint lithography (SFIL) is an attractive method for printing sub-100 nm geometries. Relative to other imprinting processes SFIL has the advantage that the template is

transparent, thereby facilitating conventional overlay techniques. In addition, the imprint process is performed at low pressures and room temperature, which minimizes magnification and distortion errors [1].

Early template fabrication schemes started with a $6 \times 6 \times 0.25''$ conventional photomask plate and used established Cr and phase shift etch processes to define features in the glass substrate [2]. Although sub-100 nm geometries were demonstrated, critical dimension (CD) losses during the etching of the thick Cr layer etch make the fabrication scheme more difficult for $1 \times$ templates [3]. It is not unusual, for example to see etch biases as large as 100 nm [4]. The purpose of this work is to investigate alternative processes for defining features on an SFIL template.

The first method considered using a much thinner (< 20 nm) layer of Cr as a hard mask. Thinner layers still suppress charging during the e-beam exposure of the template, and have the advantage that CD losses encountered during the pattern transfer through the Cr are minimized. Because the etch selectivity of SiO_2 to Cr is better than 18:1 in a fluorine based process, a sub-20 nm Cr layer is sufficient as a hard mask during the etching of the glass substrate. The second fabrication scheme attempts to address some of the weaknesses associated with a solid glass substrate. Because there is no conductive layer on the final template, SEM and defect inspection are compromised. By incorporating a conductive and transparent layer of indium tin oxide (ITO) on the glass substrate, charging is suppressed during inspection, and the transparent nature of the final template is not lost.

2. Experimental details

In order to quickly establish baseline conditions, all experiments were run on either 100 mm Pyrex 7740 wafers or 150 mm quartz wafers. NEB-22 negative resist was exposed on a Leica VB6 system operating at 100 kV. The resist process used has been described previously [5]. Cr was deposited in an MRC 603 DC magnetron load-locked sputtering system. A 1200-W, 35-mTorr process run in a single pass mode was employed. The first test samples of ITO were supplied by Silicon Quest. Those films were DC sputtered at a power of 1 kW in 100% Ar at a pressure of 8 mTorr. Subsequent development was done internally in a customized RF sputter system operating at a power of 100 W and an Ar/O_2 pressure of 6 mTorr. To further improve optical transmission and conductivity, the films were then annealed at 300 °C for 1 h in air. PECVD oxide was deposited in a Novellus Concept 1 system at a temperature of 250 °C. All pattern transfer experiments were performed in a Unaxis VLR system. A chlorine and oxygen mixture was used to etch the Cr films. A CHF_3-based etch was used to pattern transfer either the PECVD oxide or the quartz substrates.

CD measurements and top down micrographs were taken with a Hitachi S7800 CD-SEM equipped with a cold cathode source and an automated pattern recognition system. The repeatability of the CD-SEM is 3.5 nm (3σ) for line measurements and 1.4 nm (3σ) for pitch. Cross-sectioned images were obtained with a Hitachi S4500 SEM operating at 5 kV.

3. Thin Cr template process

To minimize CD loss, Cr films layers as thin as 10 nm were deposited on 150 mm quartz wafers. A 180-nm thick NEB-22 resist was exposed on the VB6 and served as the hard mask for the pattern transfer through the Cr. The Cr was then used as the hard mask for the transfer of the image into the
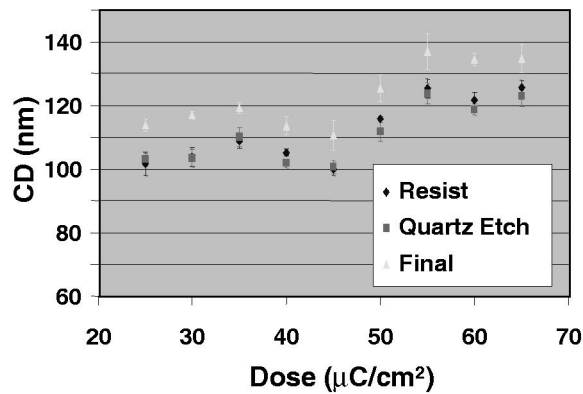
Fig. 1. CD vs. exposure dose, before and after pattern transfer. The 'resist' data are resist features on a blanket Cr film, the 'quartz etch' data are patterned resist/Cr features on the SiO_2 substrate with the pattern transferred into the substrate, and the 'final' data are with resist and Cr removed. For the latter data set it was necessary to coat the sample with a 5-nm blanket Cr film in order to measure feature dimensions with the SEM, hence the ~10 nm CD shift.
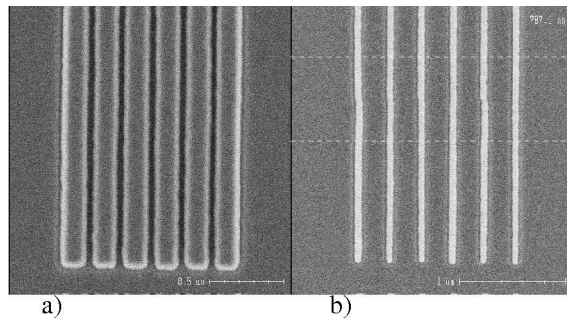

Fig. 2. The 30-nm trenches (a) and 50-nm lines (b) defined in an SFIL template. These samples were coated with a 5-nm blanket Cr layer for SEM charge dissipation. Note the stitching errors visible in (b).

quartz. Following the quartz etch, the remaining resist and Cr were stripped away, thereby producing a final template. Typical etch depths into the quartz were 100 nm.

Fig. 1 depicts the change in CD for 100 nm lines as the template was processed. No discernible shift in CD was detected after the etching of both the Cr and quartz. After stripping the resist and Cr, the template was coated with a 5-nm blanket film of Cr (to avoid charging in the SEM) and measured again. A 10-nm shift was observed, and is most likely a consequence of the blanket charge reduction layer.

Fig. 2 depicts SEM images of 30 nm trenches and 50 nm lines in the final template. These are the smallest features fabricated on an SFIL template to date.

4. Oxide/ITO template process

Although the thin Cr process successfully maintains CD control, the final template presents several problems. SEM inspection is compromised, since the quartz substrate has no means for dissipating charge. Defect inspection is also difficult, since there is no material-based contrast. It is also very
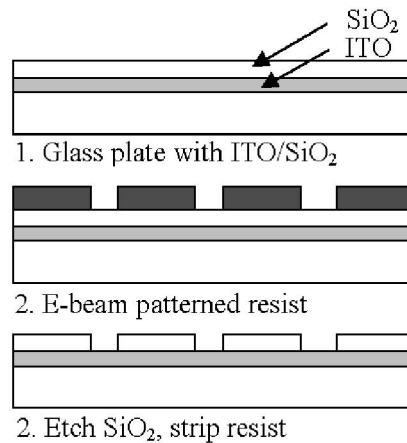
Fig. 3. Template fabrication scheme incorporating an ITO layer. The final SFIL template would have a transparent charge dissipation layer embedded in its structure, enabling end-of-line template inspection by CD-SEM.

likely that sub-50 nm templates will require electron microscopy-based defect detection schemes, which will also suffer from a lack of a charge dissipation layer [6].

To overcome these issues, we propose that a transparent conductive oxide, such as ITO, be deposited on the quartz. A PECVD oxide can then be deposited on the ITO. This oxide is coated with an e-beam resist, which is patterned and subsequently used as an etch mask for the oxide pattern transfer. Because fluorine forms no volatile products with either indium or tin, the ITO serves as an excellent etch stop. One possible fabrication scheme is depicted in Fig. 3.

Another advantage of the proposed process is improved selectivity between oxide and resist. Selectivities of better than 5:1 have been reported [7]. As a result, it should be possible to further thin the starting e-beam resist and obtain even smaller features in both the resist and final template. Cross section images (using the process described above) of dense 70 and 100 nm lines are shown in Fig. 4.

5. ITO properties

The transparent conducting oxide, ITO in this case, must satisfy a large number of criteria to be successfully implemented. The material must be transparent at 365 nm in order to polymerize the etch
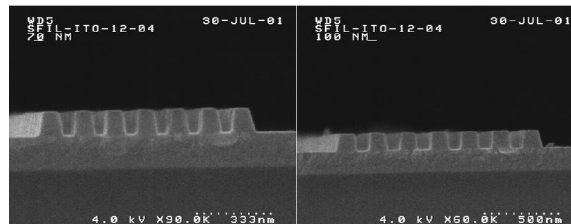

Fig. 4. Cross section SEM images of dense 70 (a) and 100 nm (b) lines. These are SiO_2 lines on a blanket ITO film—the structure is analogous to the pictorial representation in Fig. 3.
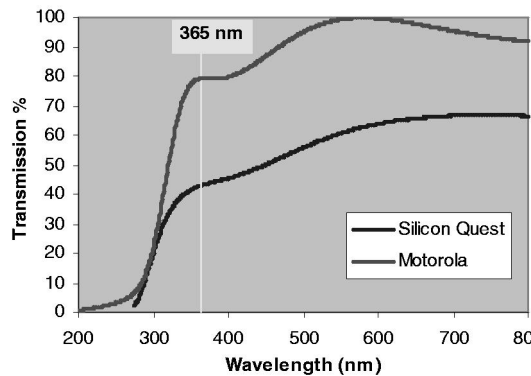
Fig. 5. Transmission spectrum for two ITO films. Initial ITO/SiO$_2$ substrates were obtained from Silicon Quest, until we could develop a process to deposit ITO at Motorola. This chart shows the superior optical transmission of the Motorola films.

barrier layer during the SFIL printing process, but be reflective enough at 780 nm to allow the VB6 laser height sensor system to locate the template surface during template exposure. Resistivity must be low enough to allow e-beam writing and template inspection without charging. Additionally, the ITO must have minimal surface roughness, possess sufficient adhesion to SiO$_2$ in order to withstand the imprint process, and be compatible with the release layer that is applied to the template prior to imprinting.

To expedite process development, ITO samples were initially obtained from Silicon Quest. A parallel effort was also started in-house to develop an ITO deposition process. Although surface roughness is superior for the externally supplied material, there was a dramatic difference in optical transmission between the two films. A comparison of 150 nm films is depicted in Fig. 5. Transmission at 365 nm differs by about a factor of two. Although 80% transmission should be more than sufficient for the imprint process, further improvements are possible by optimizing the ITO thickness and surface characteristics. It is interesting to note that although there is a large disparity in transmission, resistivity of the films are nearly identical ($\sim 5 \times 10^2$ ohms/sq).

The ITO films also appear to be sufficiently conductive. Fig. 6 depicts SEM images from an ITO-based template taken after resist development, and after oxide etch and resist strip. No blanket charge dissipation layer was applied prior to obtaining the images. The 50-nm iso-dense features were well-resolved in the resist (Fig. 6a), indicating that no local beam blurring occurred during writing. Fig. 6b depicts 100 nm dense features after oxide etch and resist strip. Line edges are well delineated and the ITO surface texture is easily observed.

6. Imprint process

A 248-nm Ultratech stepper has been converted to function as an imprint step and repeat tool, and has been detailed previously [3]. Templates and wafers are loaded and unloaded manually. Printing operations, including x–y positioning of the wafer, dispensing etch barrier liquid, z-translation of the template to close the gap between the template and wafer, UV curing of etch barrier, and controlled separation are all automated [8] and controlled with a LabVIEW interface. The system is currently
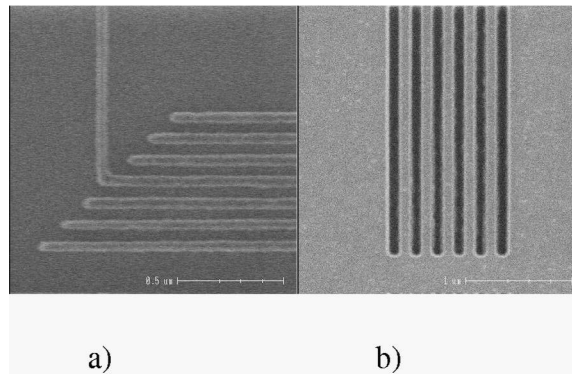
Fig. 6. SEM micrographs of an oxide/ITO template. The 50-nm features after resist development (a), demonstrating the ability for the embedded ITO film to effectively dissipate charge during e-beam exposure. The 100-nm lines/spaces after oxide etch and resist strip (b), showing that the ITO film eliminates charge build-up and provides sufficient contrast during CD-SEM inspection.
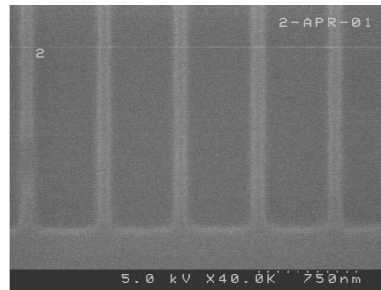

Fig. 7. Top-down SEM showing 70 nm images in the etch barrier, after imprinting. The resolution of the SFIL process seems limited by the size of the features on the imprint templates.

configured to handle 1 inch$^2 \times 0.25$ inch templates. For this study, a 0.75×0.75 inch section was cut from a finished wafer template and attached to a 0.25-inch thick by 1 inch^2 blank quartz template with an optical adhesive. The additional handling involved in bonding the wafer pieces to quartz blanks did not allow for good template–substrate orientation during imprinting, and thus made imprinting high-resolution features difficult, and imaging the resulting imprint pattern even more difficult. Work is underway to transfer the template fabrication processes to standard 0.25-inch thick substrate material, which will eliminate these difficulties. We believe resolution of that issue will allow imprinting of sub-50 nm features, and will show this work in a later publication.

An example of 70 nm features printed on the first test wafer are shown in Fig. 7. The features are well defined and faithfully reproduce the images of the templates.

7. Conclusions

Two methods for fabricating an SFIL template have been demonstrated. Both approaches are capable of defining features smaller than 70 nm. The oxide/ITO method is more appealing, however,

since it shows promise for eliminating charging effects, rendering the final template suitable for both SEM and defect inspection. Preliminary imprinting yielded features as small as 70 nm, and higher resolution imprints are expected in the near future as template development continues. Future work will attempt to create templates with smaller geometries and improve the ITO characteristics.

Acknowledgements

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